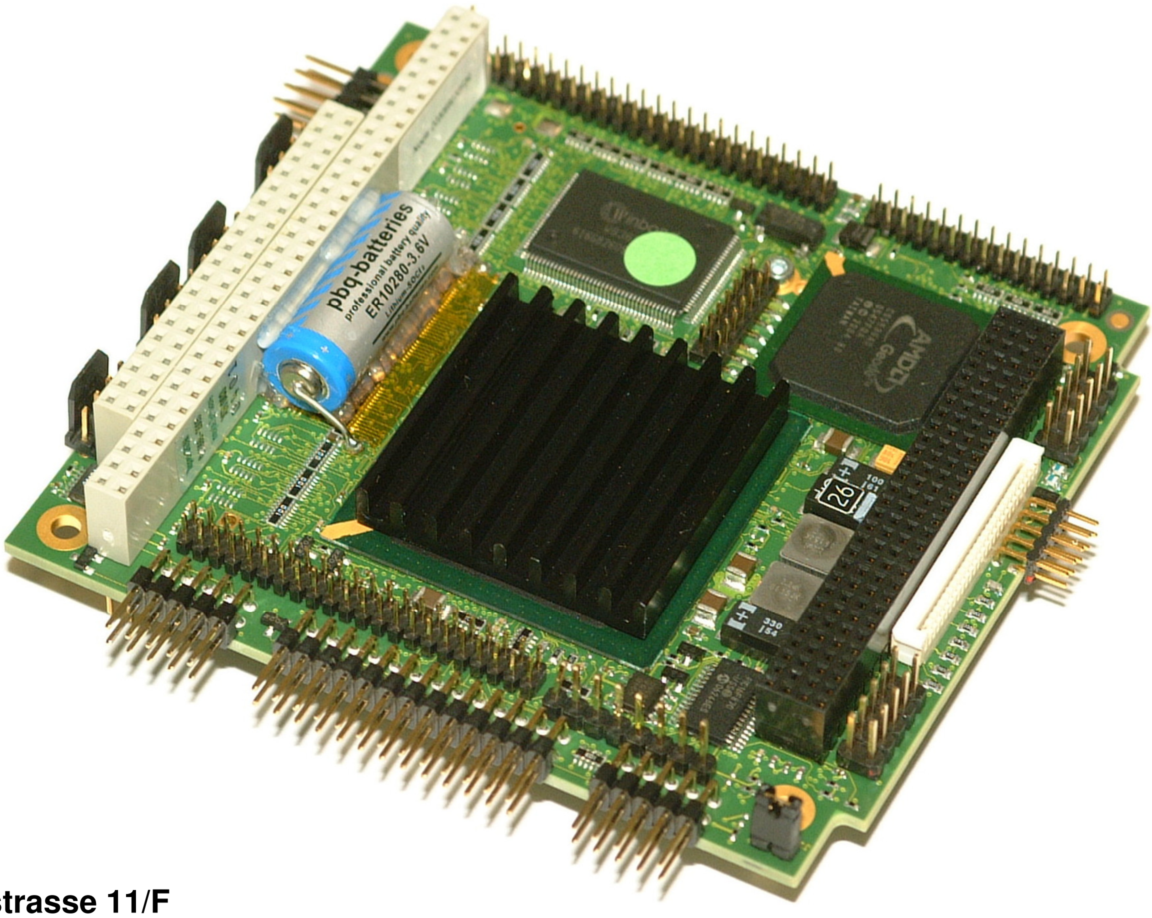
smart embedded computers

DETAILED TECHNICAL USER MANUAL FOR:

PC/104 plus

MSM800SEV/SEL
MSM800BEV
MSM800XEV/XEL



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CH - 4542 Luterbach
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Fax: ++41 (0)32 681 58 01
Email: support@digitallogic.com
Homepage: http://www.digitallogic.com

For internal use only:
File: MSM800SEV-SEL_V1.5_Detailed.doc
Path: R:\HANDBUCH\MSM\cpu_boards\MSM800\MSM800SEV-SEL_V1.5_Detailed.doc

About this Manual and How to Use It

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MICROSPACE-PC. It is for integrators and programmers of systems based on the MICROSPACE-Computer family. This manual provides instructions for installing and configuring the board, and describes the system and setup requirements. This document contains information on hardware requirements, interconnections, and details of how to program the system. Please check the Product CD for further information and manuals.

REVISION HISTORY:

Document Version	Date/Initials:	Modification: Remarks, News, Attention:
V0.1	02.2006 KUF	Initial Version
V0.2	03.2006 DAR	Preliminary Version
V0.3	03.2006 DAR	Preliminary Version
V0.4	06.2006 DAR	Preliminary Version
V1.0	07.2006 DAR	Final Release
V1.0A	07.2006 DAR	LCD connector / Flat Panel description
V1.0B	08.2006 DAR	Minor corrections, BIOS update
V1.1	10.2006 DAR	System I/O Map / Index structure, Board Version 2.1
V1.1A	11.2006 DAR	Bios V1.12, misc drawings
V1.1B	12.2006 DAR	Front Picture, Bios V1.13
V1.2	02.2007 DAR	Bios V1.14, other board versions added (not complete)
V1.2A	03.2007 DAR	Power Mgt / Bios Setup pictures Serial Port Remote Control
V1.3	04.2007 KUF	General Doc Revision/Preface additions
V1.4	05.2007 WAS/DAR KUF	Revision History format change / Filename & Path moved Previous product versions chapter added “Ext. battery connect & onboard battery removed” warning added
V1.5	***06.2007 DAR/WAS***	***Jumper7 Section 7.1 added w/Note for BIOS boot up Section 4.7.3***

Attention!
1. All information in this manual, and the product, are subject to change without prior notice.
2. Read this manual prior to installation of the product.
3. Read the security information carefully prior to installation of the product.

Table of Contents

1. PREFACE

The information contained in this manual has been carefully checked and is believed to be accurate; it is subject to change without notice. Product advances mean that some specifications may have changed. DIGITAL-LOGIC AG assumes no responsibility for any inaccuracies, or the consequences thereof, that may appear in this manual. Furthermore, DIGITAL-LOGIC AG does not accept any liability arising from the use or application of any circuit or product described herein.

1.1. Trademarks

DIGITAL-LOGIC, DIGITAL-LOGIC-Logo, MICROSPACE, and smartModule are registered trademarks owned worldwide by DIGITAL-LOGIC AG, Luterbach (Switzerland). In addition, this document may include names, company logos, and registered trademarks which are, therefore, proprietary to their respective owners.

1.2. Disclaimer

DIGITAL-LOGIC AG makes no representations or warranties with respect to the contents of this manual, and specifically disclaims any implied warranty of merchantability or fitness, for any particular purpose. DIGITAL-LOGIC AG shall, under no circumstances, be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage.

1.3. Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements wherever possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

1.4. Who should use this Product

- Electrical engineers with know-how in PC-technology.
- Because of the complexity and the variability of PC-technology, we cannot guarantee that the product will work in any particular situation or set-up. Our technical support will try to help you find a solution.
- Pay attention to electrostatic discharges; use a CMOS protected workplace.
- Power supply must be OFF when working on the board or connecting any cables or devices.

1.5. Recycling Information

All components within this product fulfill the requirements of the RoHS (Restriction of Hazardous Substances Directive). The product is soldered with a lead free process.

1.6. Technical Support

1. Contact your local DIGITAL-LOGIC Technical Support, in your country.
2. Use the Internet Support Request form at http://support.digitallogic.ch/ → embedded products → New Support Request

Support requests are only accepted with detailed information about the product (i.e., BIOS-, Board-version)!

1.7. Limited Two Year Warranty

DIGITAL-LOGIC AG guarantees the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for two years following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original purchaser of the product and is not transferable.

During the two year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

Before returning any product for repair, direct customers of DIGITAL-LOGIC AG, Switzerland are required to register a RMA (Return Material Authorization) number in the Support Center at http://support.digitallogic.ch/

All other customers must contact their local distributors for returning defective materials.

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Nor if the user has insufficient knowledge of these technologies or has not consulted the product manuals or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

Empty batteries (external and onboard), as well as all other battery failures, are not covered by this manufacturer's limited warranty.

Except, as directly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

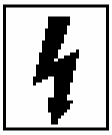
1.8. Explanation of Symbols



CE Conformity
This symbol indicates that the product described in this manual is in compliance with all applied CE standards.



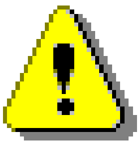
Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment.



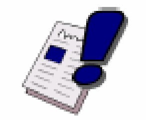
Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 32V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment



Warning, ESD Sensitive Device!
This symbol and title inform that electronic boards and their components are sensitive to Electro Static Discharge (ESD). In order to ensure product integrity at all times, care must always be taken while handling and examining this product.



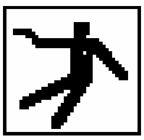
Attention!
This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your equipment.



Note...
This symbol and title emphasize aspects the user should read through carefully for his, or her, own advantage.



Warning, Heat Sensitive Device!
This symbol indicates a heat sensitive component.



Safety Instructions
This symbol shows safety instructions for the operator to follow.



This symbol warns of general hazards from mechanical, electrical, and/or chemical failure. This may endanger your life/health and/or result in damage to your equipment.

1.9. Applicable Documents and Standards

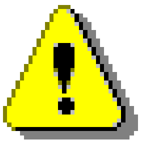
The following publications are used in conjunction with this manual. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. http://www.acpi.info/
- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/
- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. http://www.ansi.org/
- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. http://www.ansi.org/
- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://www.intel.com/labs/media/audio/
- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org/summary/sumddcci.htm
- ExpressCard Standard Release 1.0, December 2003 Copyright © 2003 PCMCIA. All rights reserved. http://www.expresscard.org/
- IEEE 802.3-2002, IEEE Standard for Information technology, Telecommunications and information exchange between systems–Local and metropolitan area networks–Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. http://www.ieee.org
- IEEE 802.3ae (Amendment to IEEE 802.3-2002), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 GB/s Operation. http://www.ieee.org
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.htm
- PCI Express Base Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Local Bus Specification Revision 2.3, March 29, 2002 Copyright © 1992, 1993, 1995, 1998, 2002 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI-104 Specification, Version V1.0, November 2003. All rights reserved. http://www.pc104.org
- PICMG® Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/
- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc, Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/

- Smart Battery Data Specification Revision 1.1, December 11, 1998. www.sbs-forum.org
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, Power-Smart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/
- Universal Serial Bus Specification Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc., Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved. http://www.usb.org/

1.10. For Your Safety

Your new DIGITAL-LOGIC product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long, fault-free life. However, this life expectancy can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and for the correct operation of your new DIGITAL-LOGIC product, please comply with the following guidelines.



Attention!
All work on this device must only be carried out by sufficiently skilled personnel.



Caution, Electric Shock!
Before installing your new DIGITAL-LOGIC product, always ensure that your mains power is switched off. This applies also to the installation of piggybacks or peripherals. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltage before performing work.



Warning, ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. In order to ensure product integrity at all times, be careful during all handling and examinations of this product.

1.11. RoHS Commitment

DIGITAL-LOGIC AG is committed to develop and produce environmentally friendly products according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC) and the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) established by the European Union. The RoHS directive was adopted in February 2003 by the European Union and came into effect on July 1, 2006. It is not a law but a directive, which restricts the use of six hazardous materials in the manufacturing of various types of electronic and electrical equipment. It is closely linked with the Waste Electrical and Electronic Equipment Directive (WEEE) 2002/96/EC, which has set targets for collection, recycling and recovery of electrical goods and is part of a legislative initiative to solve the problem of huge amounts of toxic e-waste.

Each European Union member state is adopting its own enforcement and implementation policies using the directive as a guide. Therefore, there could be as many different versions of the law as there are states in the EU. Additionally, non-EU countries like China, Japan, or states in the U.S. such as California may have their own regulations for green products, which are similar, but not identical, to the RoHS directive.

RoHS is often referred to as the "lead-free" directive but it restricts the use of the following substances:

- Lead
- Mercury
- Cadmium
- Chromium VI
- PBB and PBDE

The maximum allowable concentration of any of the above mentioned substances is 0.1% (except for Cadmium, which is limited to 0.01%) by weight of homogeneous material. This means that the limits do not apply to the weight of the finished product, or even to a component but to any single substance that could (theoretically) be separated mechanically.

1.11.1. RoHS Compatible Product Design

All DIGITAL-LOGIC standard products comply with RoHS legislation.

Since July 1, 2006, there has been a strict adherence to the use of RoHS compliant electronic and mechanical components during the design-in phase of all DIGITAL-LOGIC standard products.

1.11.2. RoHS Compliant Production Process

DIGITAL-LOGIC selects external suppliers that are capable of producing RoHS compliant devices. These capabilities are verified by:

1. A confirmation from the supplier indicating that their production processes and resulting devices are RoHS compliant.
2. If there is any doubt of the RoHS compliancy, the concentration of the previously mentioned substances in a produced device will be measured. These measurements are carried out by an accredited laboratory.

1.11.3. WEEE Application

The WEEE directive is closely related to the RoHS directive and applies to the following devices:

- Large and small household appliances
- IT equipment
- Telecommunications equipment (although infrastructure equipment is exempt in some countries)
- Consumer equipment
- Lighting equipment – including light bulbs
- Electronic and electrical tools
- Toys, leisure and sports equipment
- Automatic dispensers

It does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company that brings the product to market, as defined in the directive. Components and sub-assemblies are not subject to product compliance. In other words, since DIGITAL-LOGIC does not deliver ready-made products to end users the WEEE directive is not applicable for DIGITAL-LOGIC. Users are nevertheless encouraged to properly recycle all electronic products that have reached the end of their life cycle.

2. OVERVIEW

2.1. Standard Features

The MICROSPACE PC/104 is a miniaturized modular device incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

- Powerful Geode™ LX-800 500MHz
- BIOS ROM
- Timers, DMA
- Real-time clock with CMOS-RAM and battery buffer (external/onboard)
- LPT1 parallel port
- COM1-, COM2-RS2332 serial port
- Speaker interface
- AT-keyboard interface or PS/2-keyboard interface
- Floppy disk interface
- AT-IDE hard disk interface
- VGA/LCD video interface
- PC/104 ISA Bus
- PC104+ PCI Bus (option)
- PS/2 mouse interface
- 4 Channel USB 2.0
- Optional: Onboard CF socket Type II
- Single 5V supply
- EEPROM for setup and configuration
- UL approved parts
- Watchdog

2.2. Unique Features MSM800SEV/SEL

The MSM800SEV/SEL includes all standard PC/AT functions plus unique enhancements, such as:

- LAN Ethernet, INTEL 82551ER (or on request [optional] 82551QM)
- LPC to ISA Bridge
- SODIMM DDR-Memory holder (128-1024MByte)

2.3. Unique Features MSM800BEV/BEL

The MSM800BEV includes all standard PC/AT functions plus unique enhancements, such as:

- LAN Ethernet, INTEL 82551ER (or on request [optional] 82551QM)
- PCI to ISA Bridge for full ISA support. Needs one PCI load/resource.
- SODIMM DDR-Memory holder (128-1024MByte)

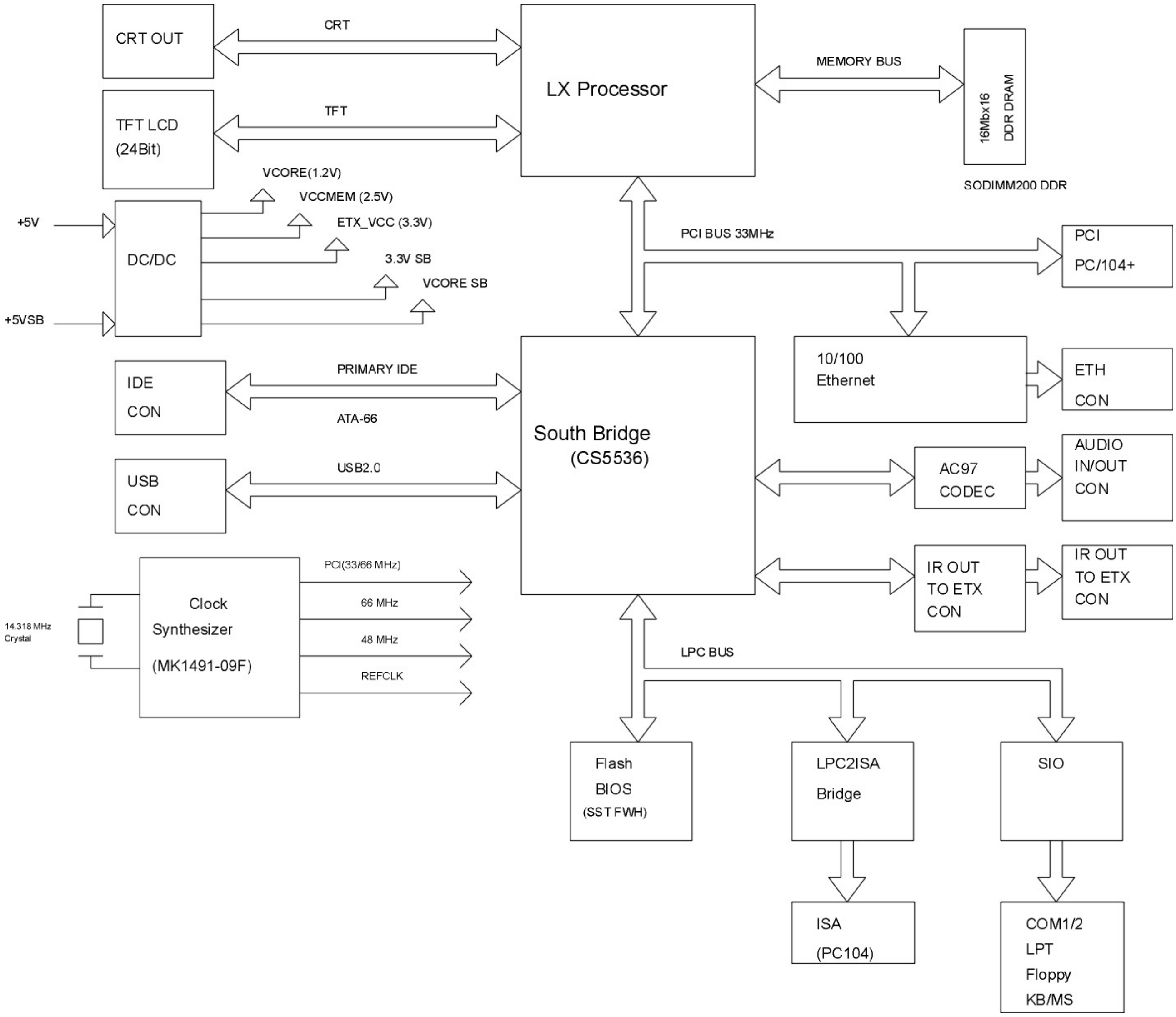
2.4. Unique Features MSM800XEV/XEL

The MSM800XEV includes all standard PC/AT functions plus unique enhancements, such as:

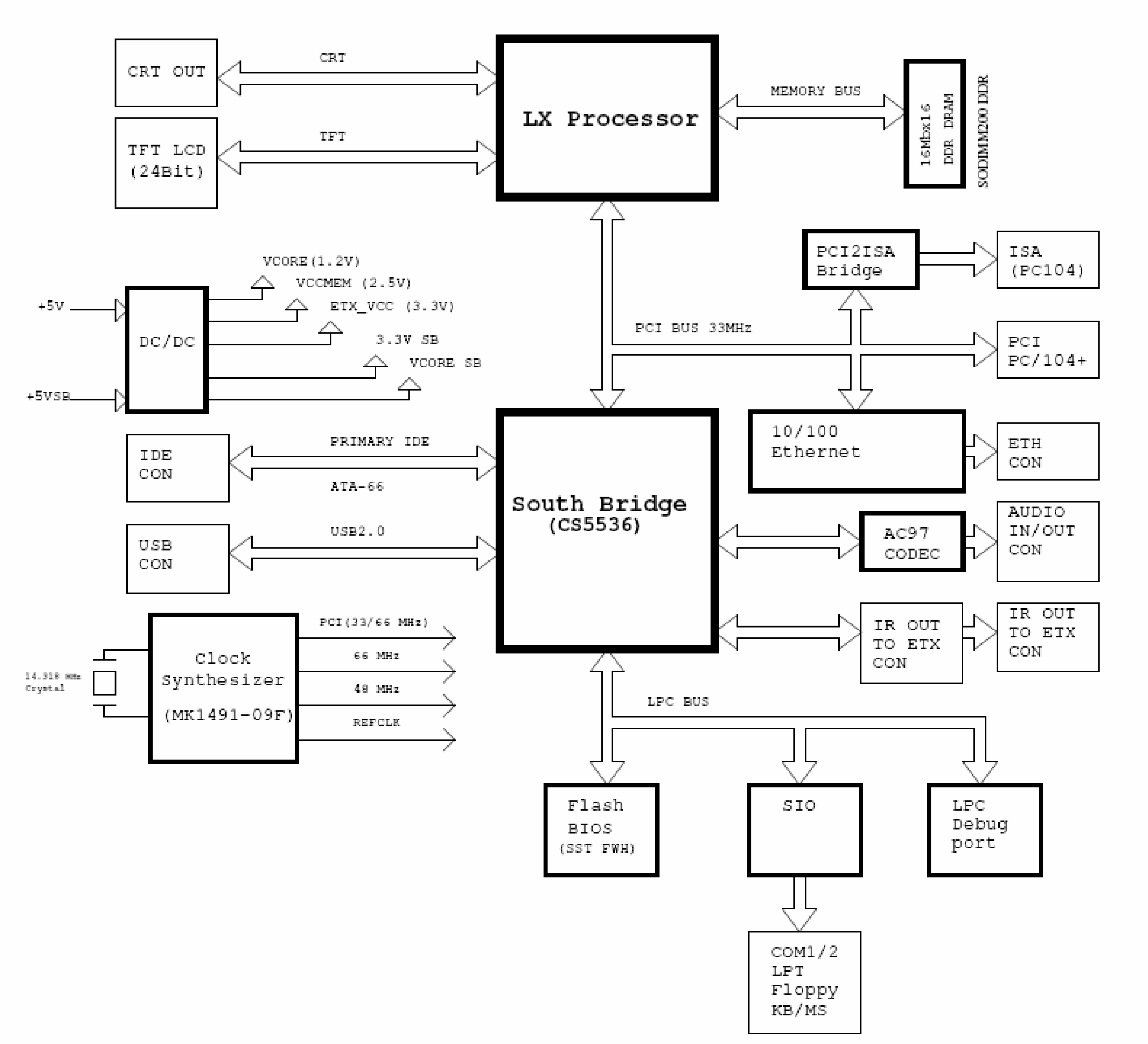
- LAN Ethernet, INTEL 82551ER (or on request [optional] 82551QM)
- PCI to ISA Bridge for full ISA support. Needs one PCI load/resource.
- Soldered 256MByte onboard DDR-RAM

2.5. Block Diagrams

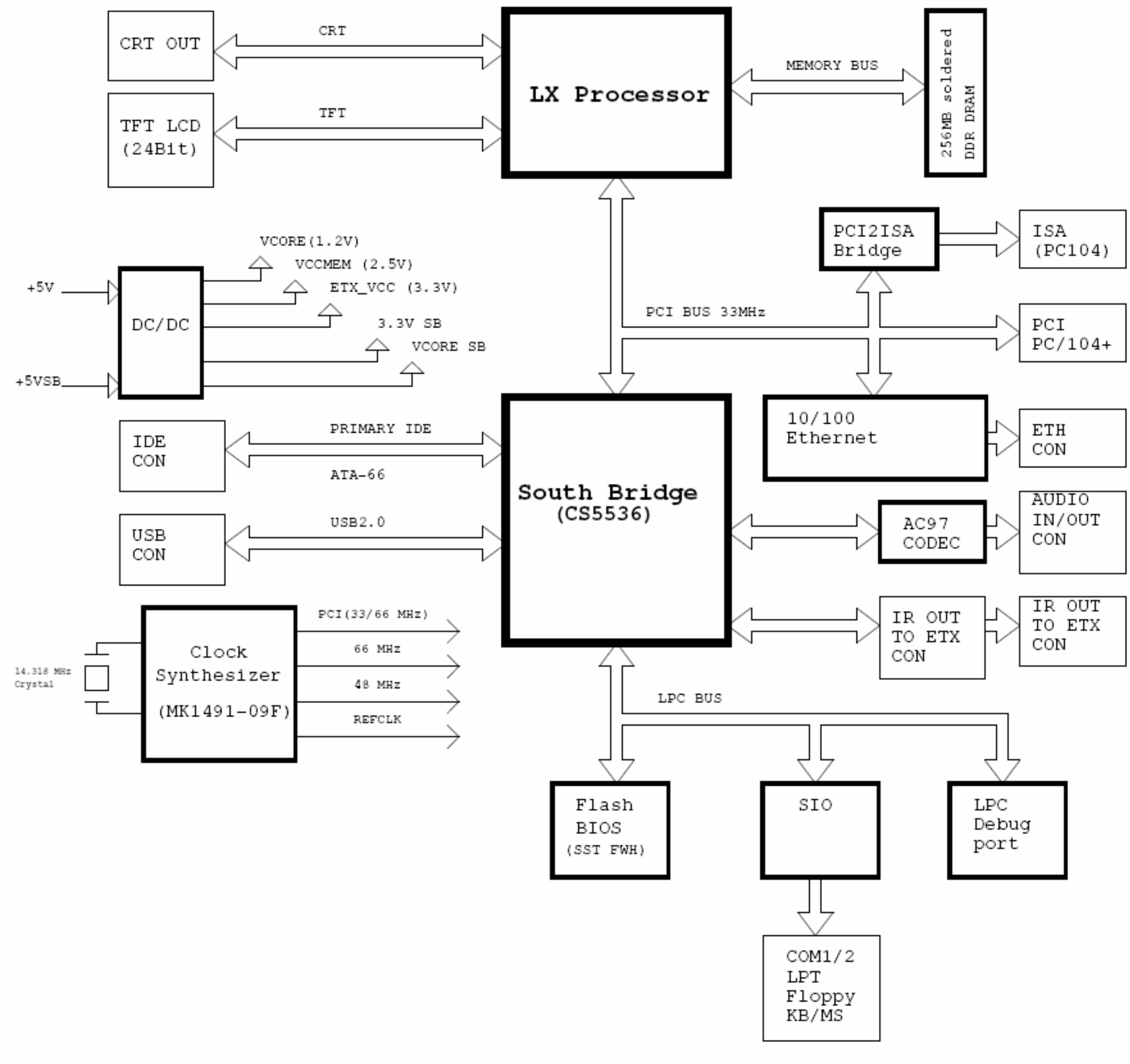
2.5.1. MSM800SEV



2.5.2. MSM800BEV



2.5.3. MSM800XEV



2.6. MSM800 SEV/SEL, BEV/BEL, XEV/XEL Specifications

CPU	
CPU	Geode LX800
CPU Core Supply	1.8V very low powered
Mode	Real/Protected
Compatibility	8086 – P5
Word Size	32bits
Secondary Cache	–
Physical Addressing	32 lines
Virtual Addressing	16GBytes
Clock Rates	500MHz
Socket Standard	Soldered BGA

Chipset	
Northbridge	AMD LX800
Southbridge	AMD 5536
LAN	10/100MBit Intel 82C551ER
Audio	AC97 – V2.3
Firewire IEEE1394	Not onboard
Video	16MByte Video-DDRAM

Power Management	
Available since V2.0	The LX800 supports ACPI and APM Version 1.2. The following ACPI Sleep States are supported: - S1 (Standby) - S3 hot* (Suspend to RAM – wake-up only with the Power Button) - S4 (Hibernation) * there are no supplies turned off

DMA	
8237A comp.	4 channel 8bits 3 channel 16bits

Interrupts	
8259 comp.	8 + 7 levels
	PC compatible

Timers	
8254 comp.	3 programmable counter/timers

Memory	
MSM800SEV/SEL/BEV MSM800SEV/SEL	SODIMM200pin DDR PC2700 333MHz 128-1024Mbyte Soldered onboard 256Mbyte DDR-RAM

Video	
Controller	MSM800SEV
BUS	32bit high speed 33MHz PCI Bus
Enhanced BIOS	VGA/LCD BIOS
Memory	2-254MByte shared RAM
CRT-Monitor	VGA, SVGA up to 1920x1440
Flat panel	TFT 3.3V 18/24bit up to 1600x1200
Controller modes	CRT only; flat panel only; or simultaneous CRT and flat panel
Video input	no
Drivers	WIN2000, XP

Mass Storage	
FD:	Floppy disk interface, for max. 1 floppy with 26pin connector
HD:	E-IDE interface, AT-type, for max. 2 hard disks, 44pin connector, for 1.3, 1.8 and 2.5" hard disks with 44 pins IDE

Standard AT Interfaces						
Serial	**Name**	**FIFO**	**IRQs**	**Addr.**	**Standard**	**Option**
	COM1 COM2	yes yes	IRQ4 IRQ3	3F8 2F8	RS232C RS232C	
	(Baud rates: 50-115 KBaud programmable)					
Parallel	LPT1 printer interface mode: SPP(output), EPP (bidir.) (Centronics)					
Keyboard	AT or PS/2 –keyboard					
Mouse	PS/2					
Speaker	0.1 W output drive					
RTC	Integrated into the chipset, RTC with CMOS-RAM 256Byte					
Backup current	<5 µA					
Non-chargeable Battery MSM800SEV/BEV/XEV MSM800SEL/BEL/XEL	 3.6V Lithium 400mAh internally or externally connected External 3.6V Lithium battery needed					

BUS	
PC/104plus	IEEE-996 standard ISA bus, buffered MSM800SEV/SEL: 8bit and limited 16bit support MSM800BEV/BEL/XEV/XEL: full 16bit ISA support
Clock	8MHz defined by the Geode

USB	
USB	2.0
Transfer rate	400MBps, 12.5MBps/1.5MBps
Channels	4

Peripheral Extension	
ISA	With PC/104 BUS MSM800SEV/SEL: with ISA 16bit DMA limitation MSM800BEV/BEL/XEV/XEL: no ISA limitation
PCI	With PC/104*plus* BUS MSM800SEV/SEL: 3 slots – max. 3 master devices MSM800BEV/BEL/XEV/XEL: 2 slots – max. 2 master devices

Power Supply	
Working	5 Volts ± 5%
Power Rise Time	Unspecified
Power consumption	MSM800SEV V2.1 with HD, MS/KB (PS/2), CRT Monitor Windows XP Desktop: type 7.5-10W
Standby power consumption	MSM800SEV/SEL/BEV: Windows Standby: 2.5W (without MS/KB wake-up function) Windows Standby: 4.5W (with PS/2 wake-up function)

Physical Characteristics	
Dimensions	Length: 91mm Depth: 96mm Height: 25mm
Weight	170gr
PCB Thickness	1.6mm / 0.0625 inches nominal
PCB Layer	Multilayer

Operating Environment	
Relative humidity	5-90% non-condensing
Vibration	5 to 2000Hz, 0.1G
Shock	1 G
Temperature	MSM800SEV/BEV/XEV*: Operating: Standard version: -25°C to +70°C Extended version: -40°C to +85°C Storage: -55°C to +85°C * = with passive cooler MSM800SEL/BEL/XEL**: Operating: Standard version: 0°C to +60°C Storage: -55°C to +85°C ** = without passive cooler

EMI / EMC (IEC1131-2 refer MIL 461/462)	
ESD Electro Static Discharge	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 Metallic protection needed Separate ground layer included 15 kV single peak
REF Radiated Electromagnetic Field	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. (not tested)
EFT Electric Fast Transient (Burst)	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 ohms, Ts=5ns Grade 2: 1kV Supply, 500 I/O, 5kHz
SIR Surge Immunity Requirements	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2kV, 6 pulse/minute I/O: 500V, 2 pulse/minute FD, CRT: none
High-frequency Radiation	EN55022

Compatibility	
MSM800SEV/BEV/XEV/SEL/BEL/XEL	Mechanically compatible to our MSMx86 Boards and to all other PC/104 boards

All information is subject to change without notice.

2.7. Examples of Ordering Codes

Part / Option	Part Nr.	Description
MSM800SEL	802105	Low cost version without: RTC-battery or heat sink
MSM800SEV	802100	Standard version with: LPC-Bridge
MSM800BEV	802110	Standard version with: full ISA-16bit support and PCI-ISA-Bridge
MSM800XEL	802125	Low cost soldered RAM version without: RTC-battery, heat sink or PCI-ISA-Bridge
MSM800XEV	802120	Standard soldered RAM version with: full ISA-16bit support and PCI-ISA-Bridge
Option -L+	807006	PC/104-*Plus* with long connector
Option -P+	807005	PC/104-*Plus* with short connector
Option -CF	807007	CompactFlash socket (without Option -L)
MSM800-CKCON	803035	MSM800 PC/104-cable kit
MSFLOPPY	891001	3.5" Micro-floppy drive (26pin)
MSFDCK	802600	Micro-floppy cable (26pin)
MSM800-LANCON	803046	LAN cable with connector print
MSM800-DVICON	803042	DVI-D interface
MSM800-LVDSCON	803044	LVDS interface
MSM800DK	802118	Development kit

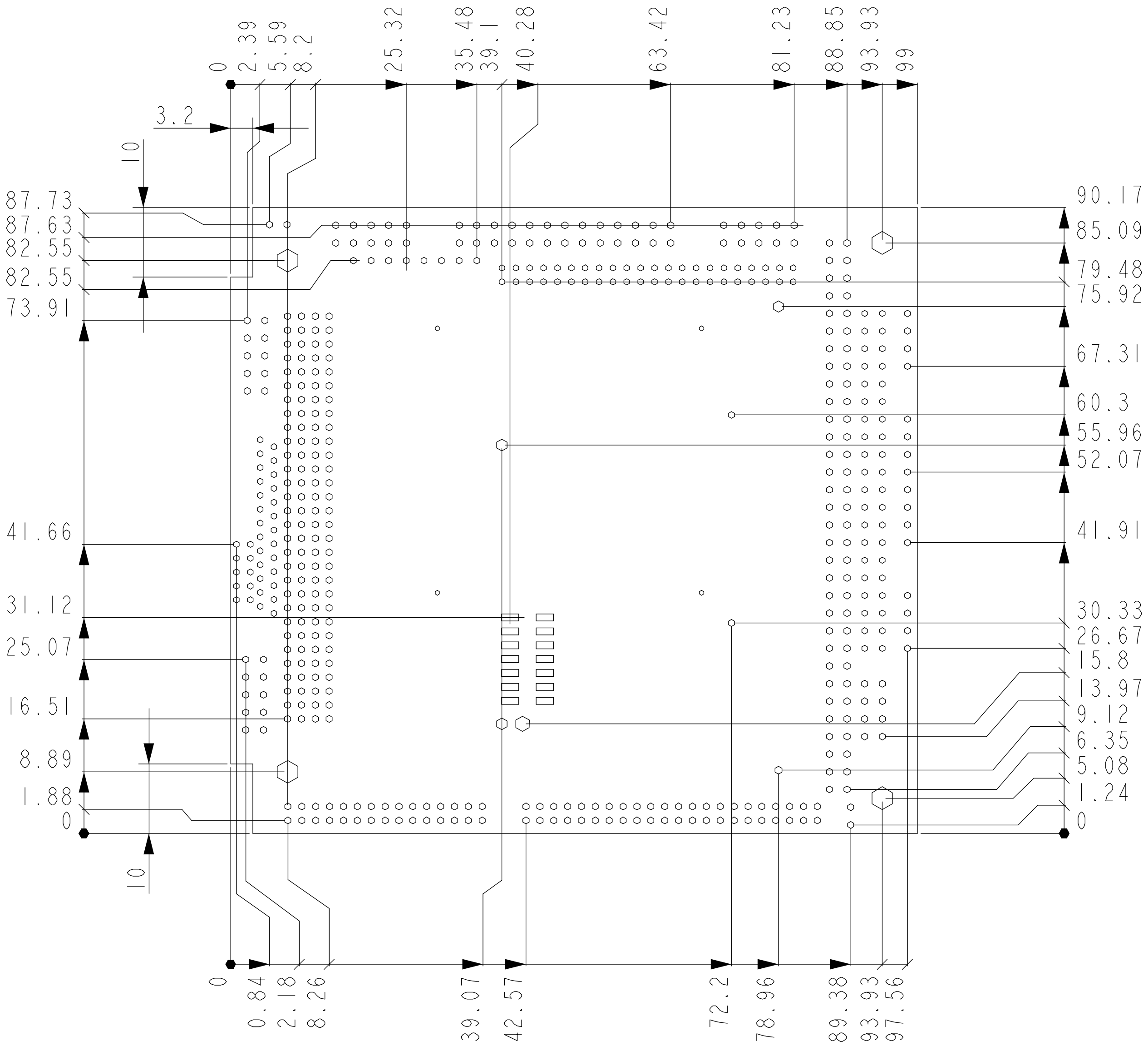
These are only examples; for current ordering codes, please see the current price list.

2.8. Dimensions and Diagrams

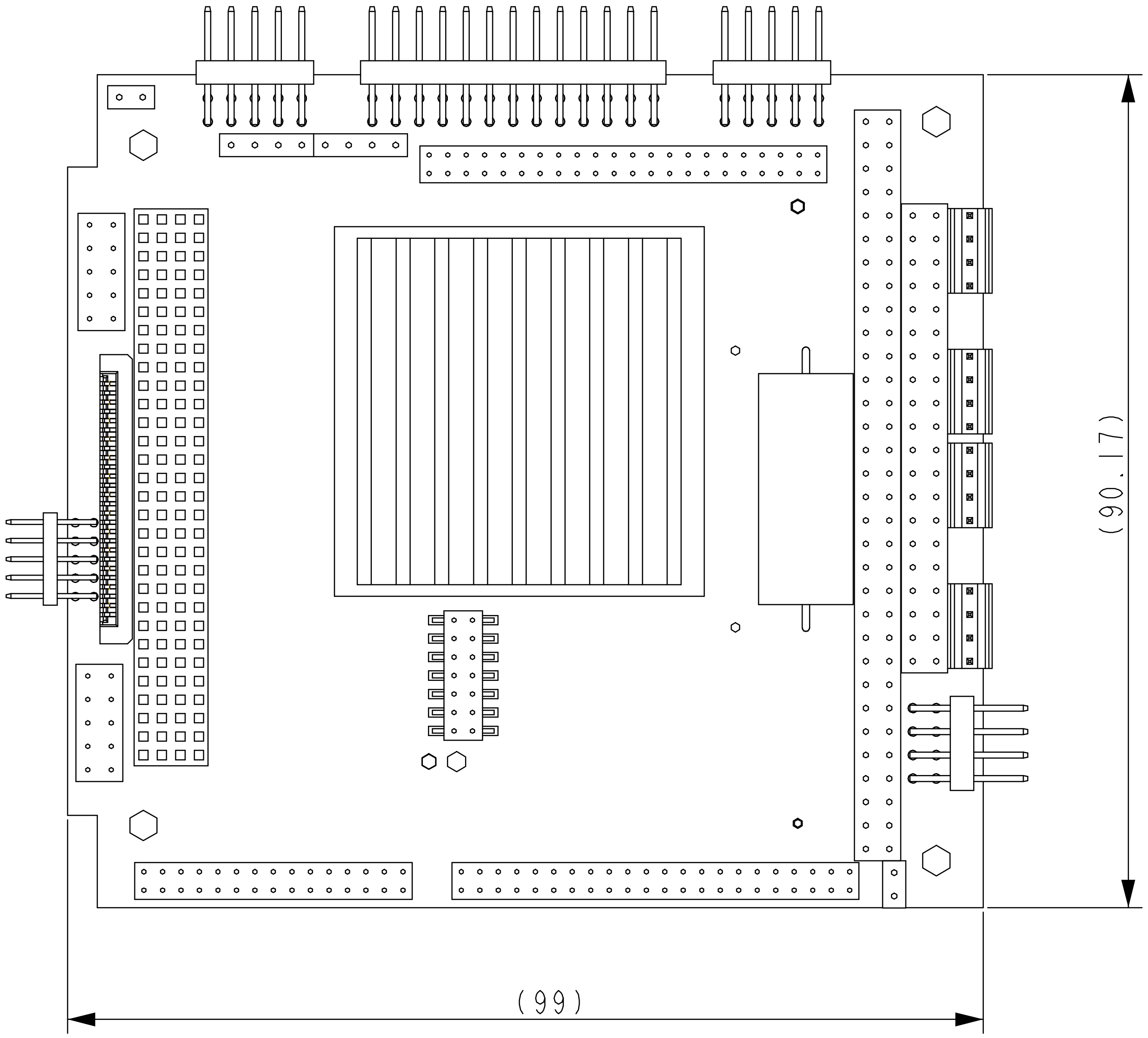
2.8.1. MSM800SEV/SEL/BEV/XEV/XEL V2.0/2.1

Board / Version	Unit:	Tolerance:	Date / Author
MSM800SEV V2.0/2.1	mm (millimeter)	+ / - 0.1mm	25.10.2006 / BRR

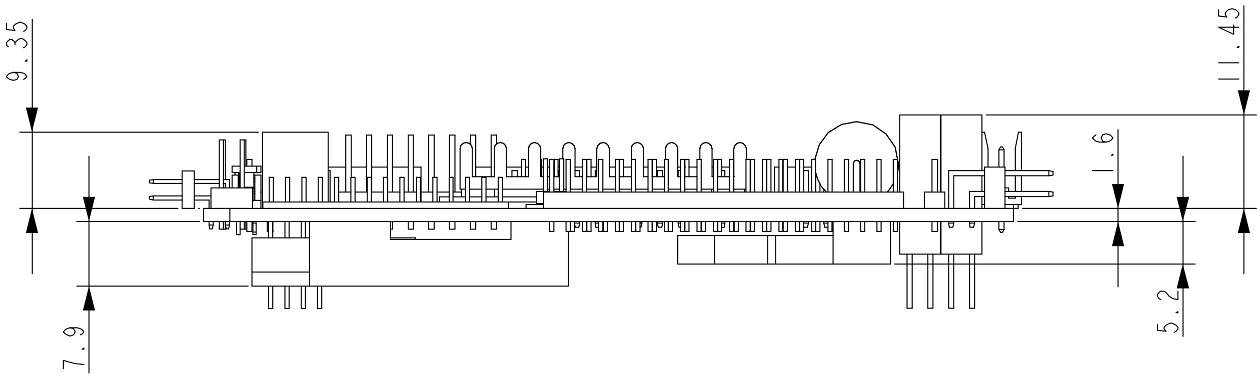
Board Dimensions



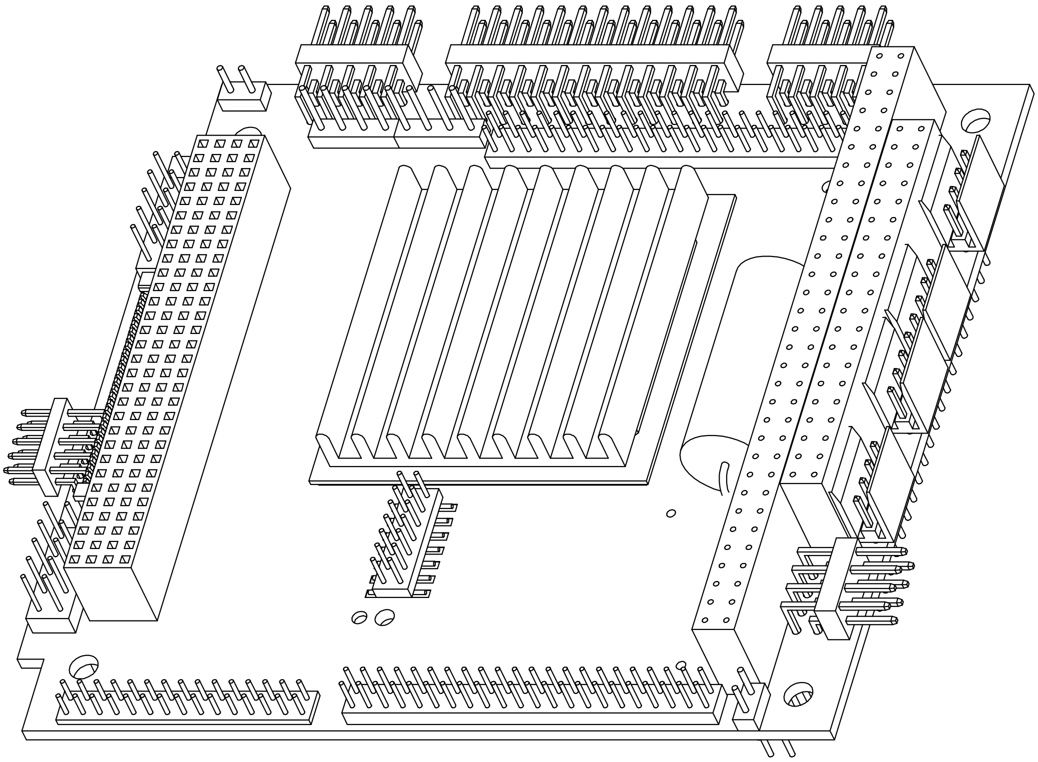
Top of board with heat sink and battery (SEV/BEV only)



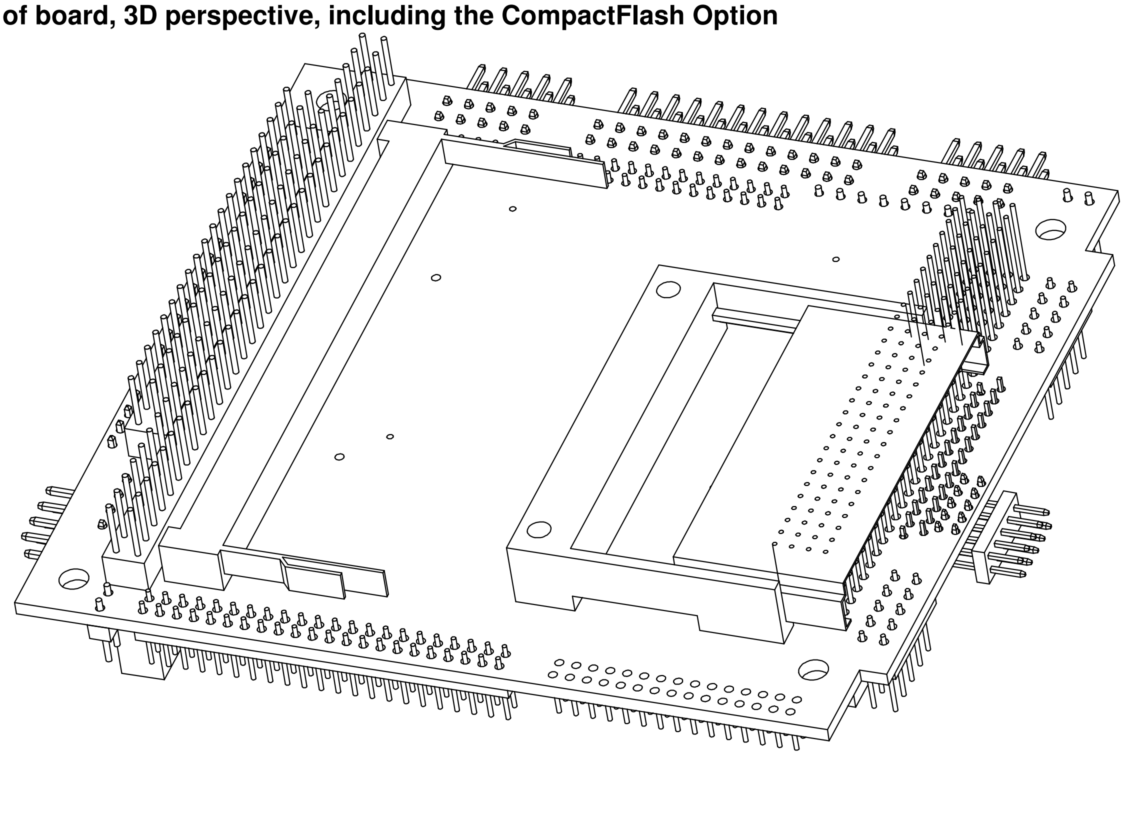
Board profile with heat sink and battery (SEV/BEV only)



Top of board with heat sink and battery, 3D perspective (SEV/VEB/XEV only)

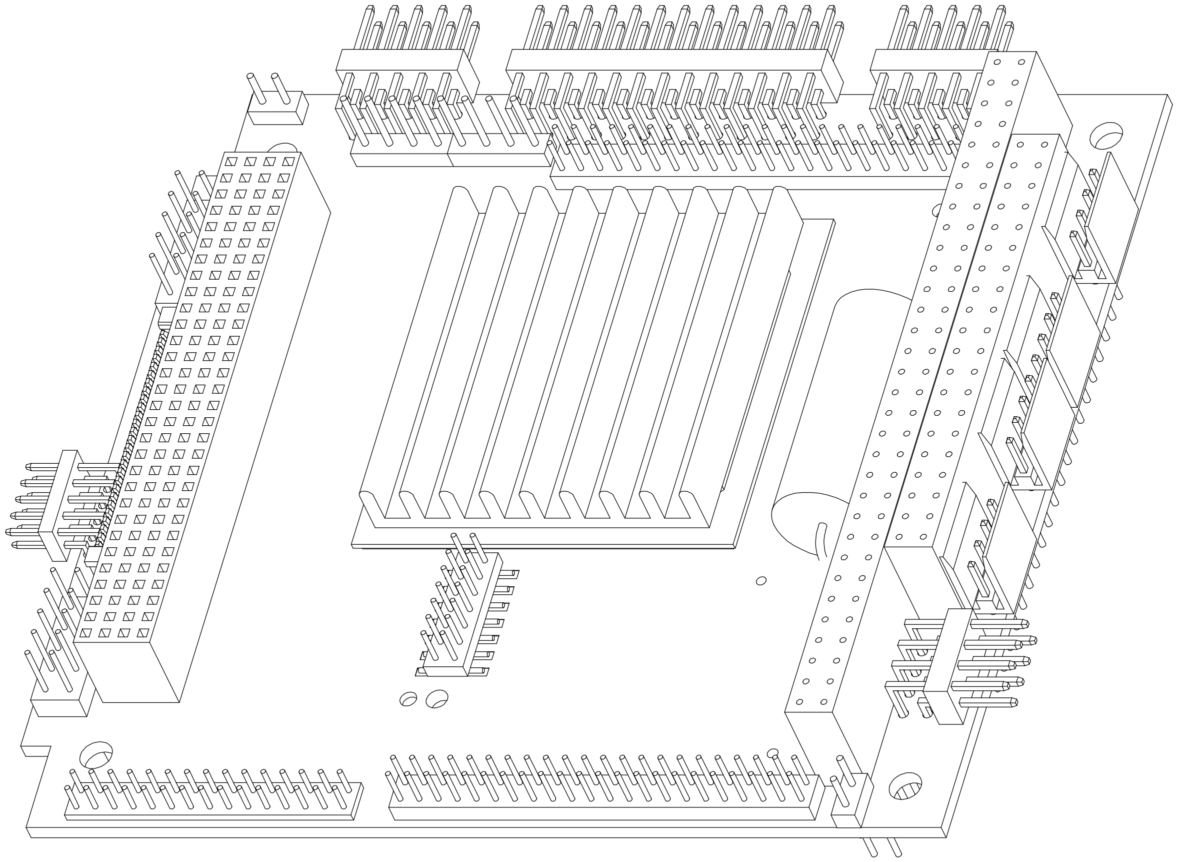


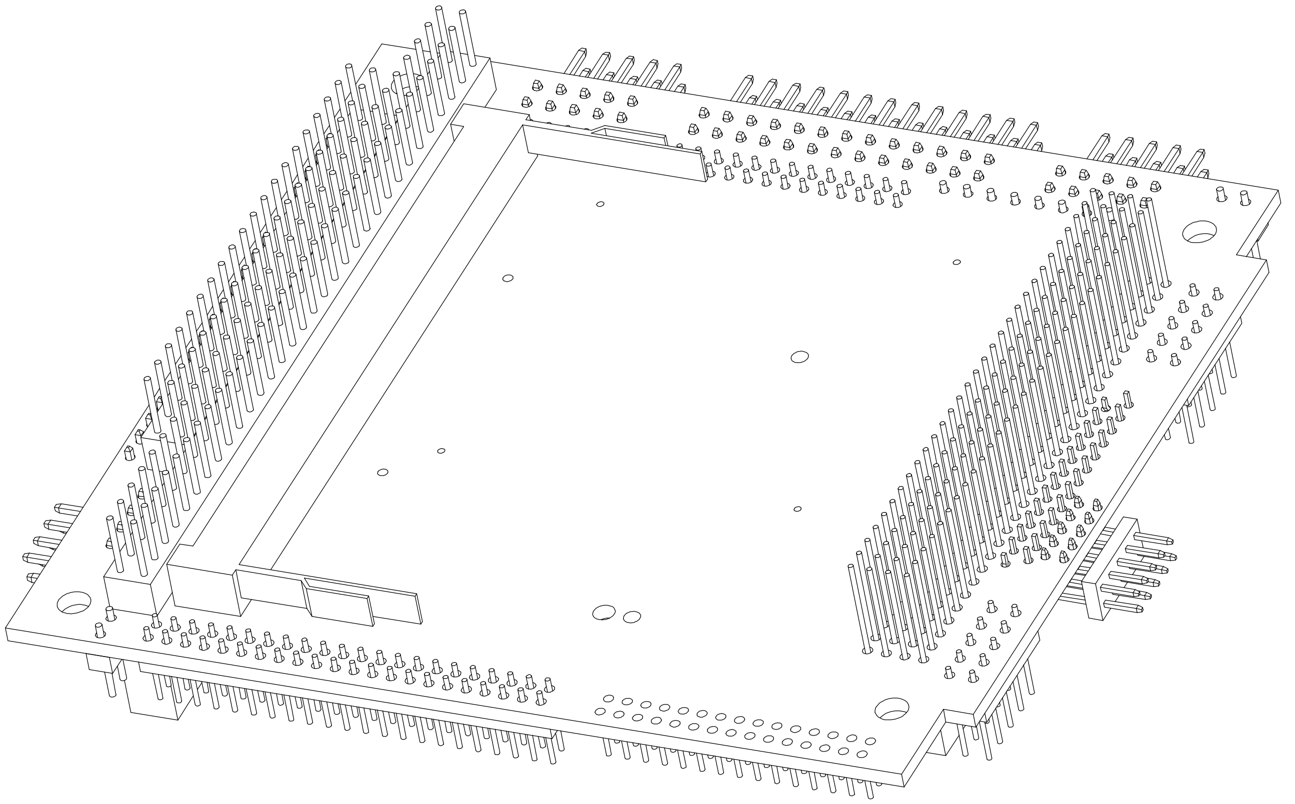
Bottom of board, 3D perspective, including the CompactFlash Option



MSM800SEV/BEV, 3D perspective

Top of Board

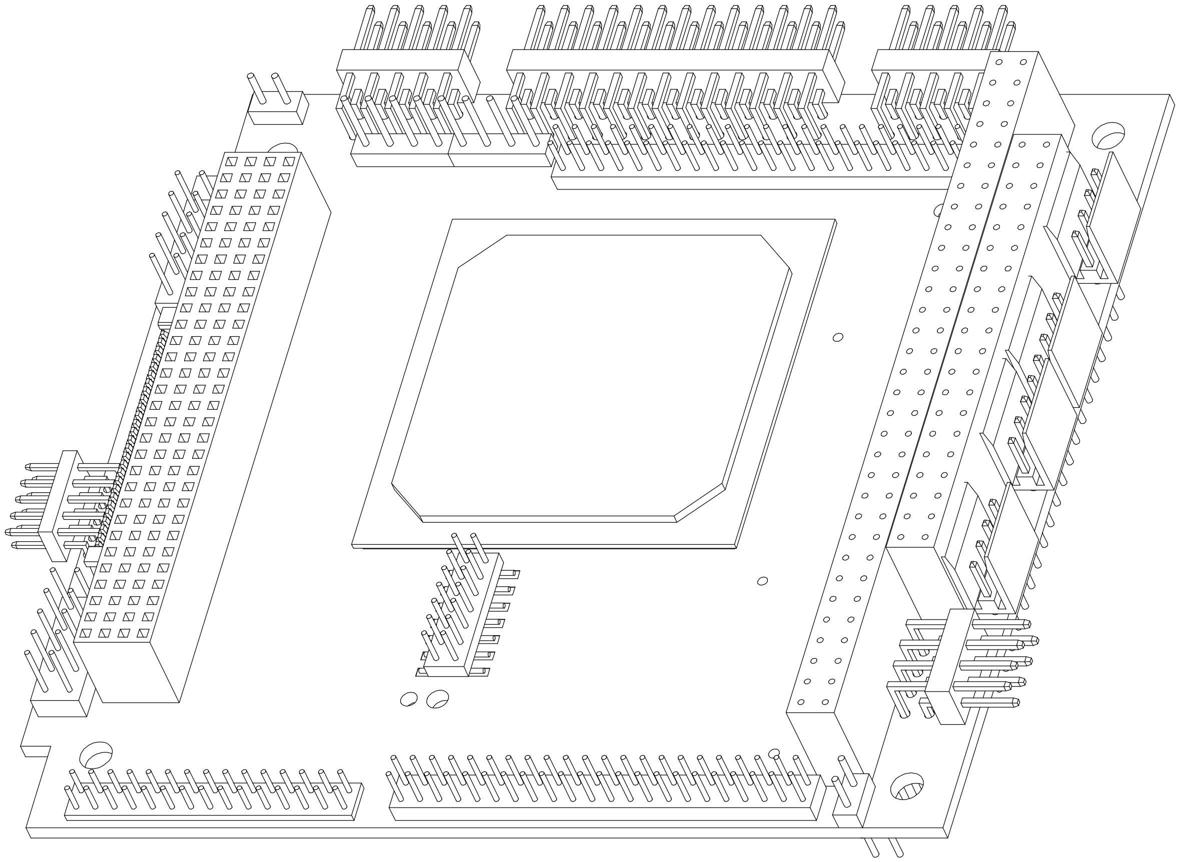


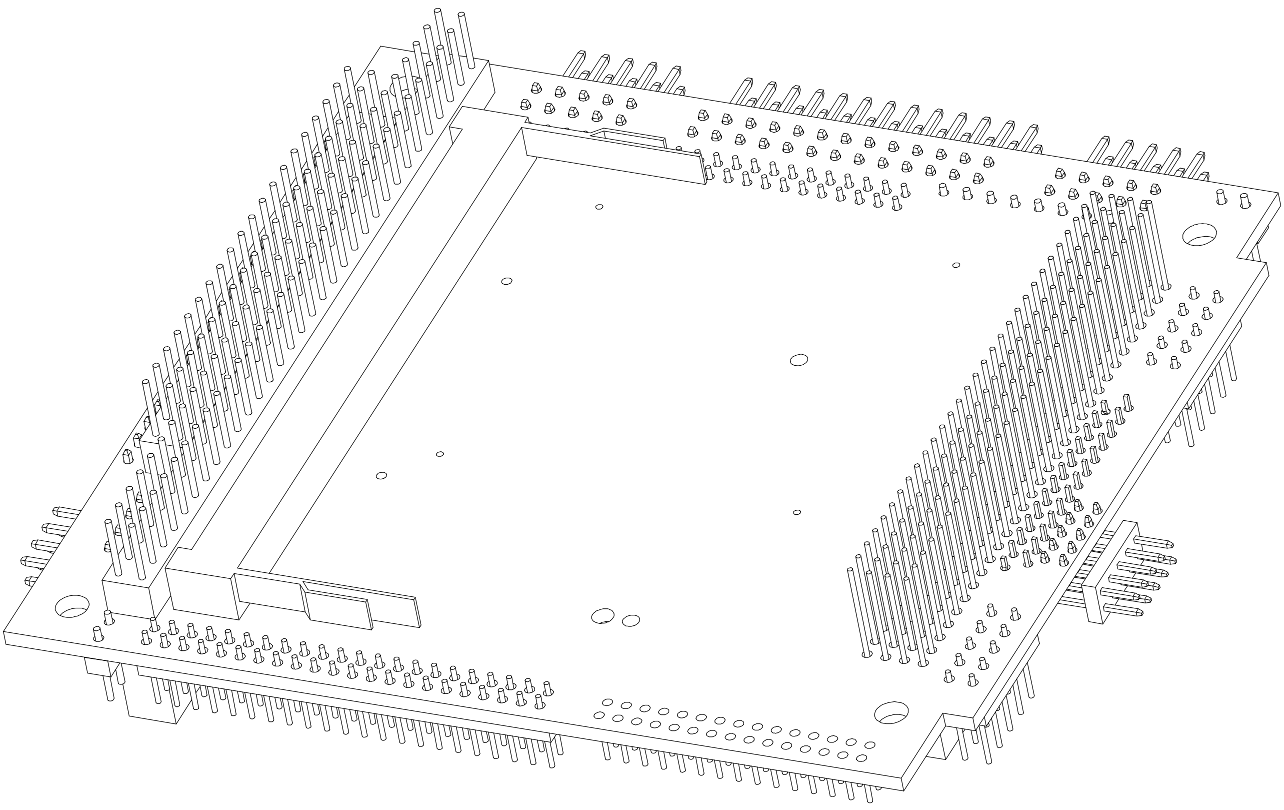


Bottom of board

MSM800SEL, 3D perspective

Top of board

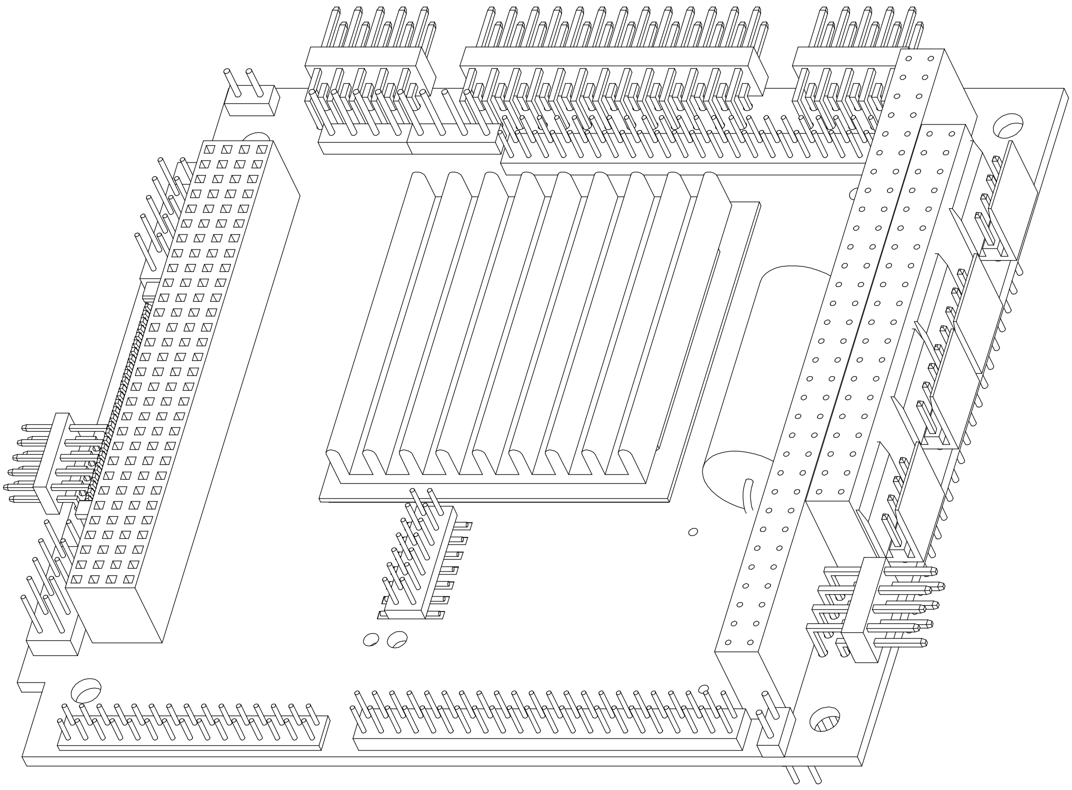


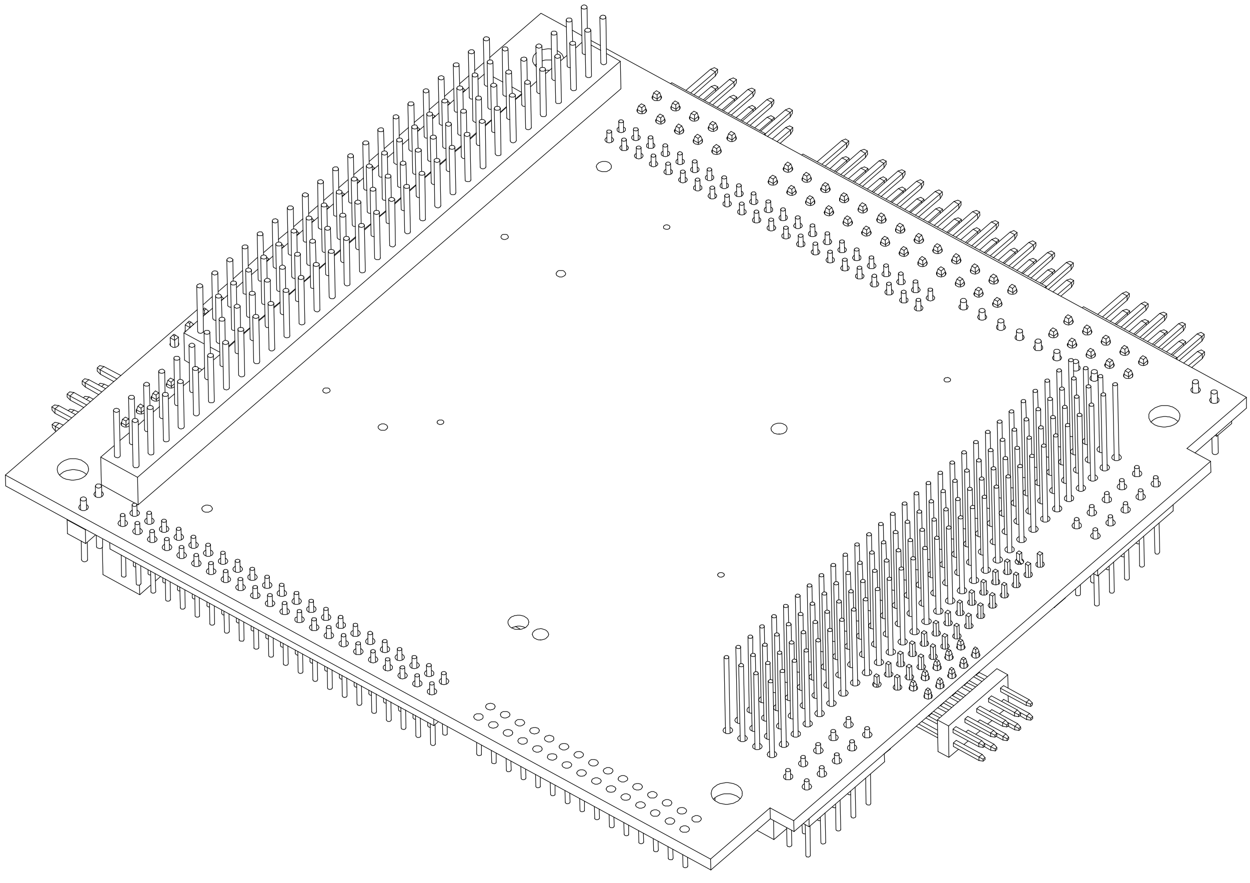


Bottom of board

MSM800XEV, 3D perspective

Top of board

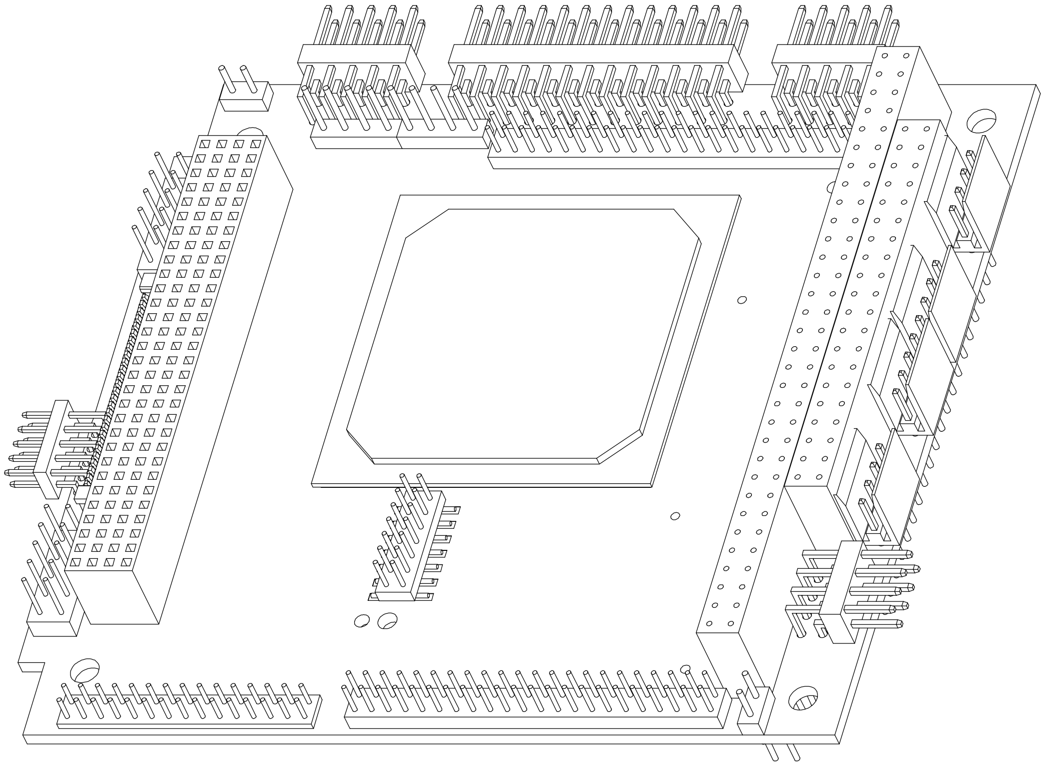


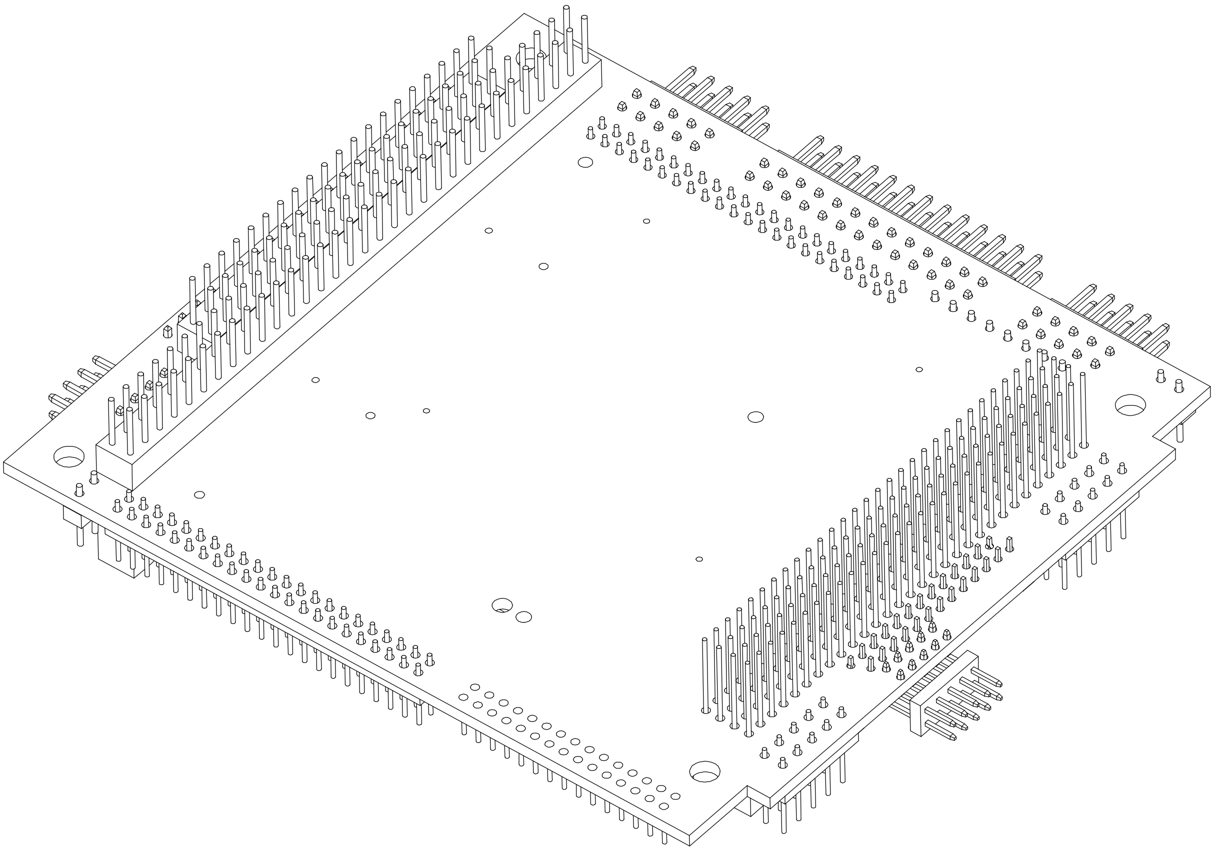


Bottom of board

MSM800XEL, 3D perspective

Top of board

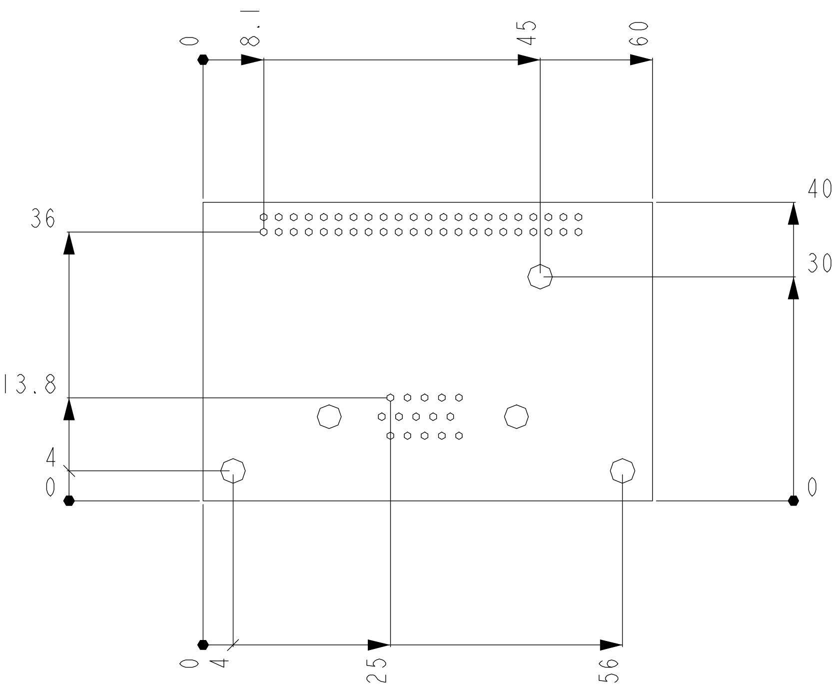


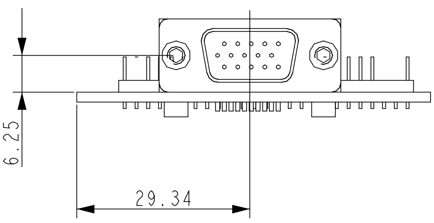


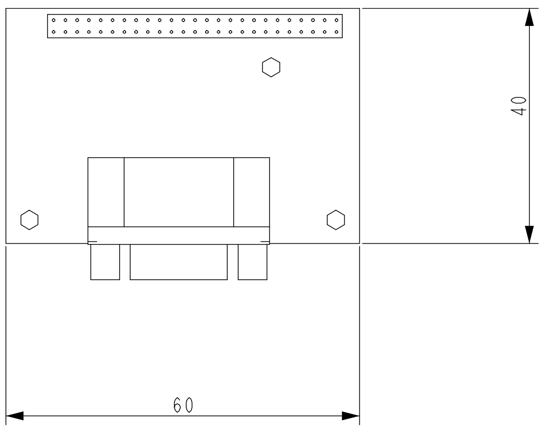
Bottom of board

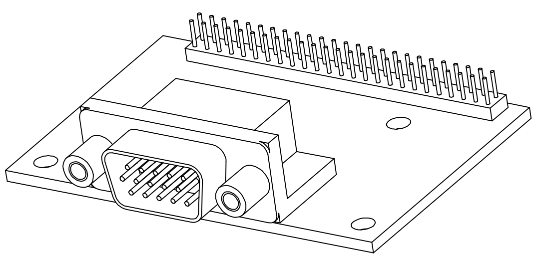
2.8.2. MSM800-LVDSCON

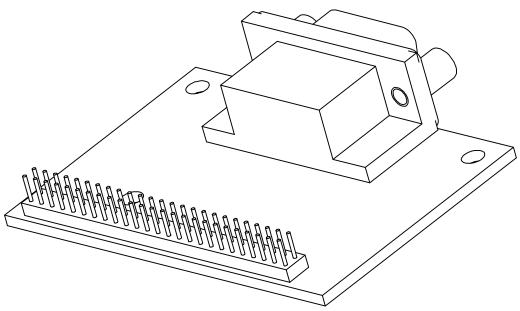
Board / Version	Unit:	Tolerance:	Date / Author
MSM800-LVDSCON V0.1	mm (millimeter)	+ / - 0.1mm	25.10.2006 / BRR





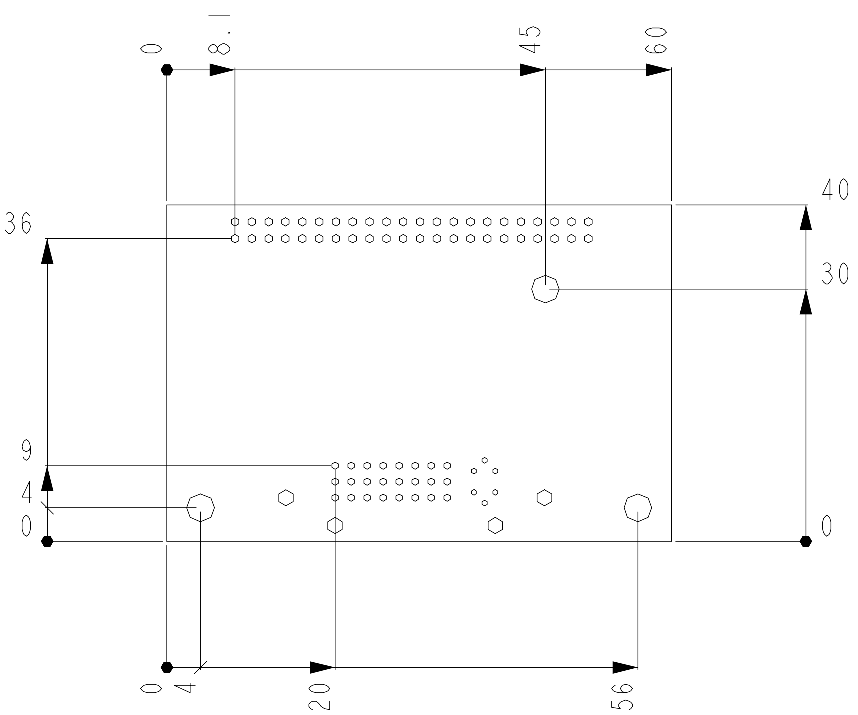


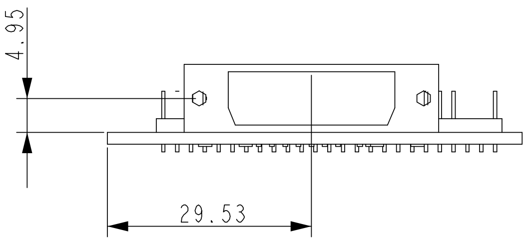


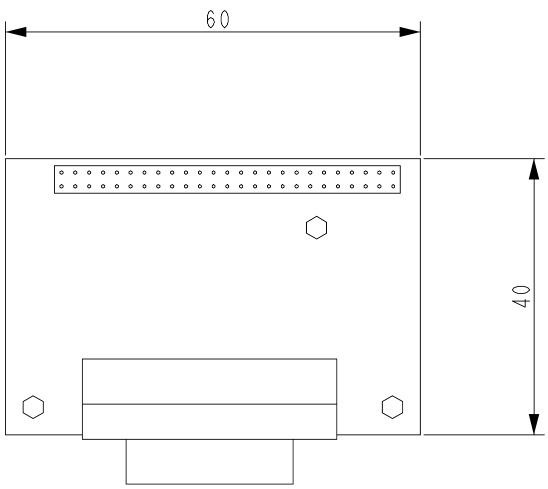


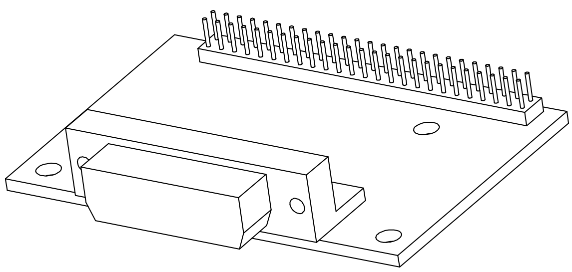
2.8.3. MSM800-DVICON

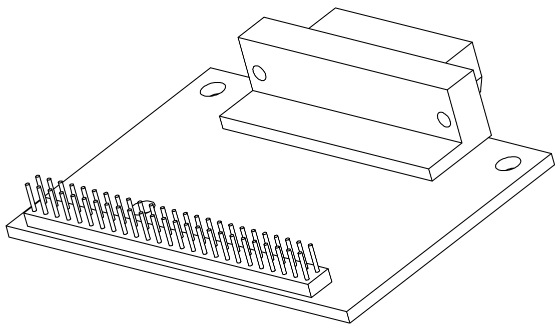
Board / Version	Unit:	Tolerance:	Date / Author
MSM800-DVICON V0.1	mm (millimeter)	+ / - 0.1mm	25.10.2006 / BRR





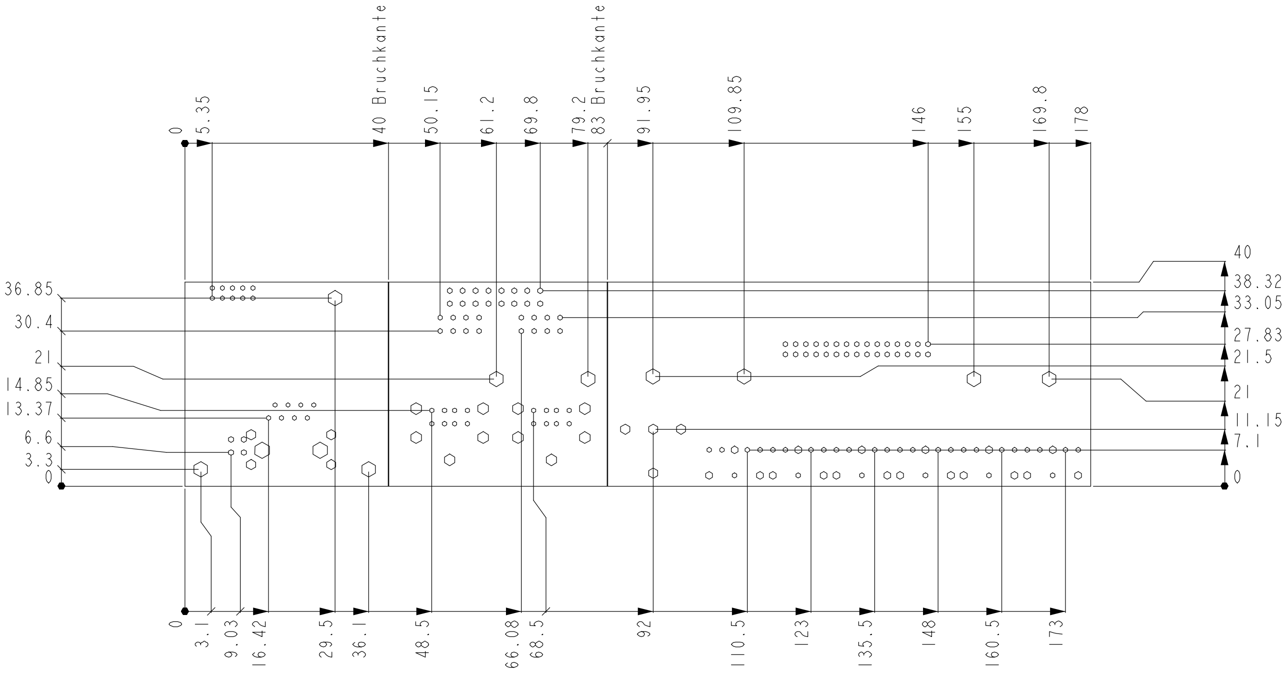


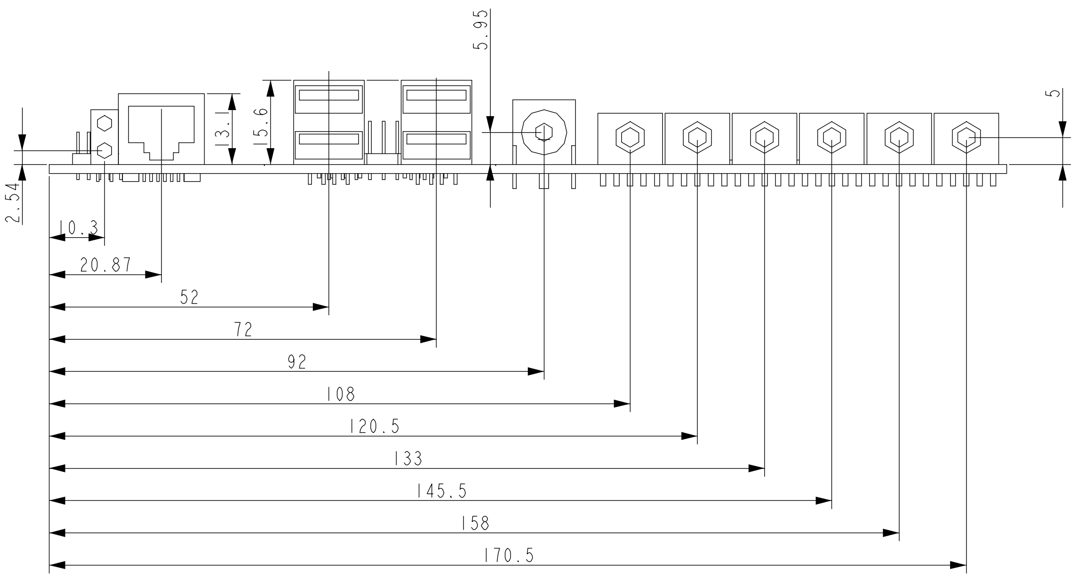


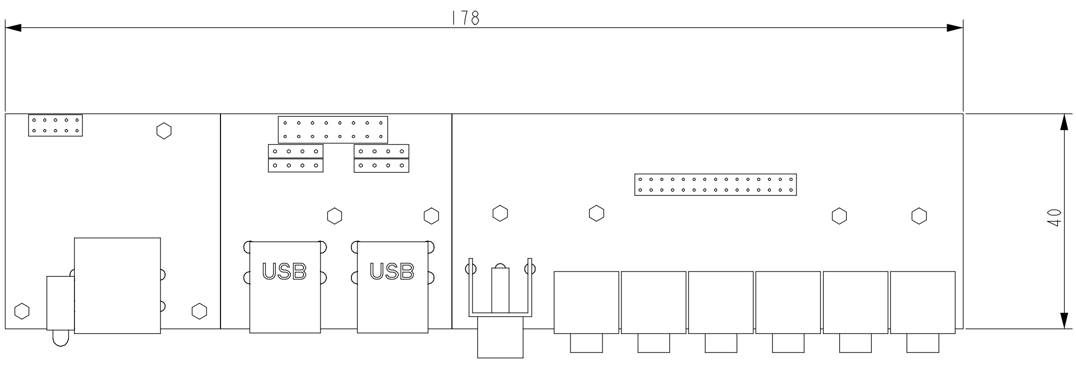


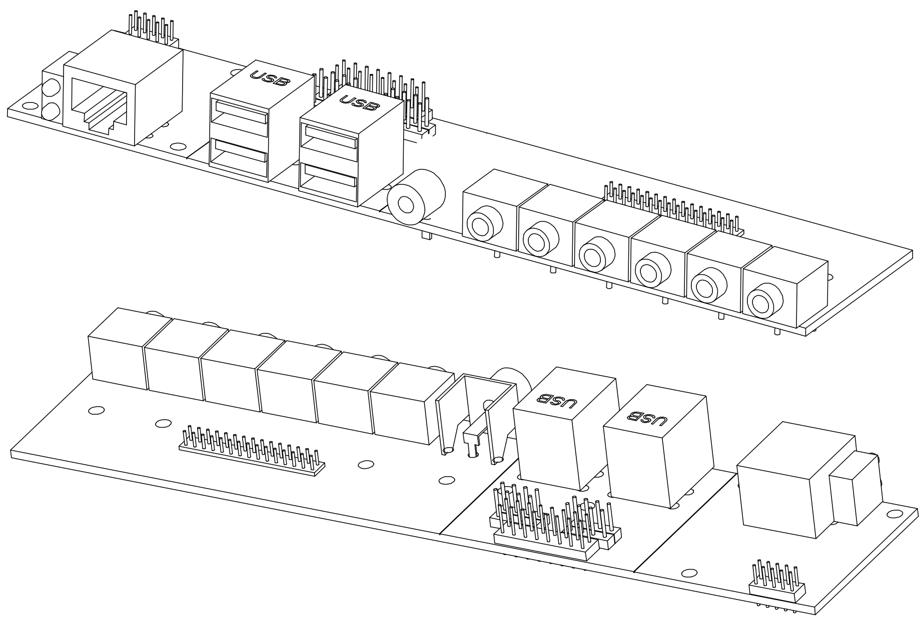
2.8.4. MSM800-CON

Board / Version	Unit:	Tolerance:	Date / Author
MSM800-CON V1.0	mm (millimeter)	+ / - 0.1mm	25.10.2006 / BRR









2.9. MSM800SEV/SEL Incompatibilities to a Standard PC/AT

2.9.1. PC104 BUS / ISA BUS

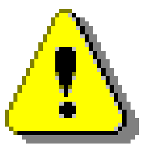
An onboard LPC to ISA-bridge makes it possible to expand the functionality of the board with additional PC/104 cards.

Unfortunately, because of the transformation from LPC to ISA it is not possible to realize a 16bit access. This does not mean that these cards cannot be used, but that the 16bit access is divided into two. Therefore the access to these cards is a little bit slower.

The LPC support the following bus cycles:

Cycle Type	Sizes Supported	Comments
Memory Read	1Byte	Optional for both LPC hosts and peripherals
Memory Write	1Byte	Optional for both LPC hosts and peripherals.
I/O Read	1Byte	Optional for peripherals.
I/O Write	1Byte	Optional for peripherals.
DMA Read	1, 2, 4Byte	Optional for peripherals.
DMA Write	1, 2, 4Byte	Optional for peripherals.
Bus Master Memory Read	1, 2, 4Byte	Optional for both LPC hosts and peripherals, but strongly recommended for hosts.
Bus Master Memory Write	1, 2, 4Byte	Optional for both LPC hosts and peripherals, but strongly recommended for hosts.
Bus Master I/O Read	1, 2, 4Byte	Optional for both LPC hosts and peripherals.
Bus Master I/O Write	1, 2, 4Byte	Optional for both LPC hosts and peripherals.
Firmware Memory Read	1, 2, 4, 128Byte	Optional for both LPC hosts and peripherals.
Firmware Memory Write	1, 2, 4Byte	Optional for both LPC hosts and peripherals.

This means, all Non-BusMaster I/O and MEM Cycles are only 8bit wide and never 16bit wide. 16bit data transfer is available in the BusMaster modus only.



Attention!
With the BEV/BEL/XEV/XEL versions, this limitation is solved by using a PCI-ISA bridge. The disadvantage is that now 2 PCI devices are onboard and there are only 2 external PCI slots available.

2.9.2. ISA-Incompatibility with ISA-PCCARD-Controller

Experience shows that ATA-Drives controlled in an ISA-PCMCIA Controller do not work.

Solution: Use a PCCARD-Controller on the PCI-Bus

2.9.3. ISA-Incompatibility with 16bit I/O Transfer with FPGA-Decoder

Our experience shows that 16bit I/O-transfers decoded with a FPGA do not always work correctly. Each case must be tested. Expect problems on odd addresses.

Solution: Use two 8bit transfers instead of one 16bit transfer. For time critical transfers we recommend using the PCI-Bus.

2.9.4. ISA-Incompatibility with 16bit Memory Transfer with FPGA-Decoder

Experience shows that 16bit Memory-transfers decoded with a FPGA do not always work correctly. Each case must be tested. Expect problems on odd addresses.

Solution: Use two 8bit transfers instead of one 16bit transfer. For time critical transfers we recommend using the PCI-Bus.

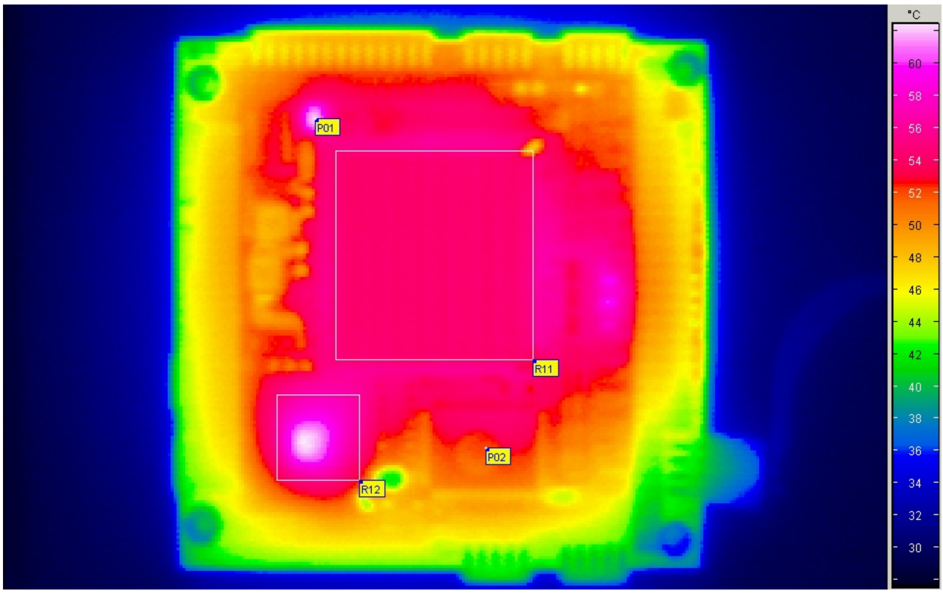
2.10. Related Application Notes

Application Notes are available at http://www.digitallogic.com → support, or on any DIGITAL-LOGIC Application CD.

#	Description

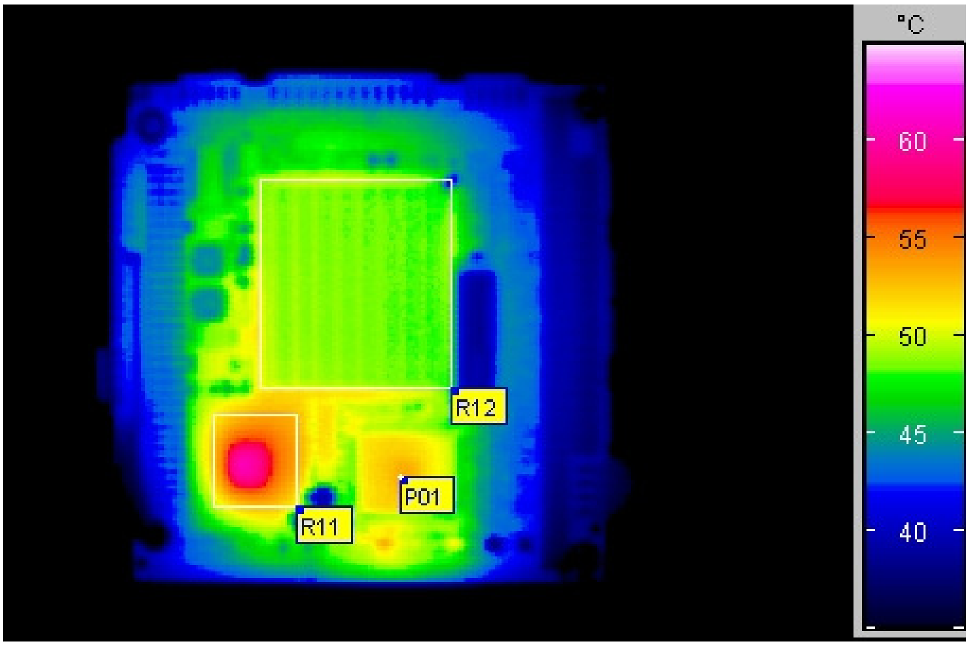
2.11. Thermoscan

MSM800SEV V1.2 with heat sink (OS: MSDOS → promt)



t [min]	f_{CPU} [MHz]	P01 [°C]	P02 [°C]	R11 [°C]	R12 [°C]
45	500	61.9	52.1	56.2	62.6

MSM800SEV V2.1 with heat sink (OS: MSDOS → promt)



t [min]	f_{CPU} [MHz]	P01 [°C]	R11 [°C]	R12 [°C]
90	500	53.1	60.5	51.1

2.12. High Frequency Radiation (to meet EN55022)

Since the PC/104 CPU modules are very highly integrated embedded computers, peripheral lines are not protected against radiation from the high frequency spectrum. To meet a typical EN55022 requirement, all peripherals that go outside of the computer case must be externally filtered.

Typical signals that must be filtered:

Keyboard:	KBCLK, KBDATA and VCC
Mouse:	MSCLK, MSDATA and VCC
COM1/2/3/4:	All serial signals must be filtered
LPT:	All parallel signals must be filtered
CRT:	Red, blue, green, hsynch and vsynch must be filtered

Typical signals that must not be filtered, since they are used internally:

IDE:	Connected to the hard disk
Floppy:	Connected to the floppy
LCD:	Connected to the internal LCD

2.12.1. For Peripheral Cables:

Use a filtered version for all DSUB connectors. Select the filter specifications carefully. Place the filtered DSUB connector directly on the front side and be sure that the shielding makes good contact with the case.

9pin	DSUB connector from AMPHENOL:	FCC17E09P	820pF
25pin	DSUB connector from AMPHENOL:	FCC17B25P	820pF

2.12.2. For Stack-Through Applications:

On each peripheral signal line that goes outside the computer case, place a serial inductivity followed by a grounded capacitor of 100pF to 1000pF. In this case, no filtered connectors are needed. Place the filter directly under or behind the onboard connector.

Serial Inductivity:	TDK HF50ACB321611-T	100MHz, 500mA, 1206 Case
Ground Capacitor:	Ceramic Capacitor with 1000pF	

2.12.3. Power Supply:

Use a current-compensated dual inductor on the 5V supply.

SIEMENS B82721-K2362-N1 with 3.6A, 0.4mH

2.13. Battery Lifetime

Note...
The RTC back-up battery is assembled onboard only for the MSM800SEV/BEV/XEV systems.

Battery specifications		**Lowest temp. -40°C**	**Nominal temp. +20°C**	**Highest temp. +85°C**
Manufacturer	pba			
Type	ER10280			
Capacity versus temp.	10uA	430mAh	400mAh	300mAh
Voltage versus temp.	10uA	3.6V	3.6V	Ca. 3.6V
Nominal values	3.6V / 400mAh @ 0.5mA / -55°C...~+85°C			

Information is taken from the datasheet.

Product	**Temperature °C**	**Battery voltage V**	**VCC (+5) switched ON µA**	**VCC (+5V) switched off µA**
Battery current	+25°C	3.6	< 1	< 4
Battery lifetime	+25°C		> 5 years	> 5 year

2.13.1. External Battery Assembly:

Note...
The MSM800SEL/BEL/XEL versions require this.

The external battery must be a lithium 3.6Volt with a capacity from 400-800mAh.

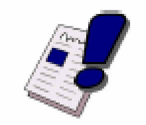
If the customer wants to connect an external battery (check for the appropriate connector in chapter 6), some precautions must be taken:

- Do not use a rechargeable battery – the battery is prohibited from charging.
- The RTC device defines a voltage level of 3-3.6V, so use an external battery within this range (inclusive of the diode which is already assembled onboard).

Attention!
For systems that already have an onboard battery (MSM800SEV/BEV/XEV): if an external battery is to be connected, then the onboard battery **must** be removed first.

3. BUS SIGNALS

3.1. PC104 Bus



Note...
Not all of the signals are available on this board (please see Chapter 6 for a description of the connectors).

AEN, output

Address Enable: used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. **low = CPU Cycle, high = DMA Cycle**

BALE, output

Address Latch Enable: provided by the bus controller and used on the system board to latch valid addresses and memory decodes from the microprocessor. This signal is used so that devices on the bus can latch LA17-23. The SA0-19 address lines latch internally according to this signal. BALE is forced high during DMA cycles.

/DACK[0, 5-7], output

DMA Acknowledge: 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQO through DRQ7). They are **active low**. This signal indicates that the DMA operation can begin.

DRQ[0, 5-7], input

DMA Requests: 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK/) line goes active. DRQO through DRQ3 will perform 8bit DMA transfers; DRQ5-7 are used for 16 accesses.

/IOCHCK, input

IOCHCK/: provides the system board with parity (error) information about memory or devices on the I/O channel. **low = parity error, high = normal operation**

IOCHRDY, input

I/O Channel Ready: pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of one clock cycle (67 nanoseconds). This signal should be held in the range of 125-15600nS. **low = wait, high = normal operation**

/IOCS16, input

I/O 16 Bit Chip Select: signals the system board that the present data transfer is a 16bit, 1 wait-state, I/0 cycle. It is derived from an address decode. /IOCS16 is **active low** and should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 20mA. The signal is driven based only on SA15-SAO (not /IOR or /IOW) when AEN is not asserted. In the 8bit I/O transfer, the default transfers a 4 wait-state cycle.

/IOR, input/output

I/O Read instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

/IOW, input/output

I/O Write: instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is **active low**.

IRQ [10, 12, 14, 15], input

These signals are used to tell the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is **raised from low to high**. The line must be held high until the microprocessor acknowledges the interrupt request.

/Master, input

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/0 channel may issue a DRQ to a DMA channel in cascade mode and receive a /DACK.

/MEMCS16, input

MEMCS16 Chip Select: signals the system board if the present data transfer is a 1 wait-state, 16bit, memory cycle. It must be derived from the decode of LA17 through LA23. /MEMCS16 should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 2OmA.

/MEMR, input/output

These signals instruct the memory devices to drive data onto the data bus. /MEMR is active on all memory read cycles. /MEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/0 channel wishes to drive /MEMR, it must have the address lines valid on the bus for one system clock period before driving /MEMR active. These signals are **active low**.

/MEMW, input/output

These signals instruct the memory devices to store the data present on the data bus. /MEMW is active in all memory read cycles. /MEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMW, it must have the address lines valid on the bus for one system clock period before driving /MEMW active. Both signals are **active low**.

OSC, output

Oscillator (OSC): a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle. OSC starts 100µs after reset is inactive.

RESETDRV, output

Reset Drive: used to reset or initiate system logic at power-up time or during a low line-voltage outage. This signal is **active high**. When the signal is active all adapters should turn off or tri-state all drivers connected to the I/O channel. This signal is driven by the permanent Master.

/REFRESH, input/output

These signals are used to indicate a refresh cycle and can be driven by a microprocessor on the I/0 channel. These signals are **active low**.

SA0-SA19, LA17 - LA23 input/output

Address bits 0 through 19 are used to address memory and I/0 devices within the system. These 20 address lines, allow access of up to 1MBytes of memory. SAO through SA19 are gated on the system bus when BALE is high and are latched on the falling edge of BALE. LA17 to LA23 are not latched and addresses the full 16MByte range. These signals are generated by the microprocessors or DMA controllers. They may also be driven by other microprocessor or DMA controllers that reside on the I/0 channel. The SA17-SA23 are always LA17-LA23 address timings for use with the MSCS16 signal. This is advanced AT96 design. The timing is selectable with jumpers LAxx or SAxx.

/SBHE, input/output

Bus High Enable (system): indicates a transfer of data on the upper byte of the data bus, XD8 through XD15. Sixteen-bit devices use /SBHE to condition data-bus buffers tied to XD8 through XD15.

SD[0-15], input/output

These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/0 devices. D0 is the least significant bit and D15 is the most significant bit. All 8bit devices on the I/O channel should use D0 through D7 for communications to the microprocessor. The 16bit devices will use D0 through D15. To support 8bit devices, the data on D8 through D15 will be gated to D0 through D7 during 8bit transfers to these devices; 16bit microprocessor transfers to 8bit devices will be converted to two 8bit transfers.

/SMEMR, input/output

These signals instruct the memory devices to drive data onto the data bus for the first MByte. /SMEMR is active on all memory read cycles. /SMEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/0 channel wishes to drive /SMEMR, it must have the address lines valid on the bus for one system clock period before driving /SMEMR active. The signal is **active low**.

/SMEMW, input/output

These signals instruct the memory devices to store the data present on the data bus for the first MByte. /SMEMW is active in all memory read cycles. /SMEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMW, it must have the address lines valid on the bus for one system clock period before driving /SMEMW active. Both signals are **active low**.

SYSCLK, output

This is an 8MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 66% duty cycle. This signal should only be used for synchronization.

TC, output

Terminal Count: provides a pulse when the terminal count for any DMA channel is reached. The TC completes a DMA-Transfer. This signal is expected by the onboard floppy disk controller. Do not use this signal, because it is internally connected to the floppy controller.

/0WS, input

The Zero Wait State (/0WS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16bit device without wait cycles, /0WS is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8bit device with a minimum of one-wait states, /OWS should be driven active one system clock after the Read or Write command is active, gated with the address decode for the device. Memory Read and Write commands to an 8bit device are active on the falling edge of the system clock. /0WS is **active low** and should be driven with an open collector or tri-state driver capable of sinking 20mA.

12V, +/- 5%

This signal is used only for the flat panel supply.

GROUND = 0V

This is used for the entire system.

VCC, +5V +/- 0.25V

This signal is used for logic and hard/floppy disk supply.

For further information about PC/104 and PC/104plus, please refer to the PC/104 Specification Manual which is available on the internet: http://www.digitallogic.com (manuals).

3.2. PC104+ Bus

AD[31:00]

Address and Data are multiplexed. A bus transaction consists of an address cycle followed by one or more data cycles.

C/BE[3:0]*

Bus Command/Byte Enables are multiplexed. During the address cycle, the command is defined. During the Data cycle, they define the byte enables.

PAR

Parity is even on AD[31:00] and C/BE[3:0]* and is required.

FRAME*
Frame is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle.

TRDY*
Target Ready indicates the selected device's ability to complete the current data cycle of the traansaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle.

IRDY*
Initiator Ready indicates the master's ability to complete the current data cycle of the transaction.

STOP*
Stop indicates the current selected device is requesting the master to stop the current transaction.

DEVSEL*
Device Select is driven by the target device when its address is decoded.

IDSEL
Initialization Device Select is used as a chip-select during configuration.

LOCK*
Lock indicates an operation that may require multiple transactions to complete.

PERR*
Parity Error is for reporting data parity errors.

SERR*
System Error is for reporting address parity errors.

REQ*
Request indicates to the arbitrator that this device desires use of the bus.

GNT*
Grant indicates to the requesting device that access has been granted.

CLK
Clock provides timing for all transactions opn the PCI bus.

RST*
Reset is used to bring PCI-specific registers to a known state.

INTA*
Interrupt A is used to request Interrupts.

INTB*
Interrupt B is used to request Interrupts only for multi-function devices.

INTC*
Interrupt C is used to request Interrupts only for multi-function devices.

INTD*
Interrupt D is used to request Interrupts only for multi-function devices.

3.3. Expansion Bus

The bus currents are as follows:

Output Signals	IOH	IOL
D0-D16	8 mA	8 mA
A0-A23	8 mA	8 mA
MR, MW, IOR, IOW, RES, ALE, AEN, C14	8 mA	8 mA
DACKx, DRQx, INTx, PSx, OPW	8 mA	8 mA

Output Signals	Logic Family	Voltage
Input Signals:	ABT-Logic ViH (min.) = 2.15 V	ABT-Logic Vil (max.) = 0.85 V

3.4. Addressing PCI Devices

3.4.1. MSM800SEV/SEL V2.1

DEVICE	IDSEL	PIRQ	#REG	#GNT	Remarks
SLOT 1	AD20	A / B / C / D	3	3	For additional cards (peripheral boards)
SLOT 2	AD21	B / C / D / A	4	4	For additional cards (peripheral boards)
SLOT 3	AD22	C / D / A / B	5	5	For additional cards (peripheral boards)
SLOT 4	AD23	D / A / B / C	-	-	For additional cards (peripheral boards)
LAN	AD29	A	0	0	Onboard devices

3.4.2. MSM800BEV/XEV/XEL V1.x

DEVICE	IDSEL	PIRQ	#REG	#GNT	Remarks
SLOT 1	AD20	A / B / C / D	3	3	For additional cards (peripheral boards)
SLOT 2	AD21	B / C / D / A	4	4	For additional cards (peripheral boards)
SLOT 3	AD22	C / D / A / B	5	5	For additional cards (peripheral boards)
SLOT 4	AD23	D / A / B / C	6	6	For additional cards (peripheral boards)
LAN	AD29	A	7	7	Onboard devices
PCI-ISA-Bridge	AD24		8	8	

4. DETAILED SYSTEM DESCRIPTION

This system has a system configuration based on the ISA architecture. Check the I/O and the Memory map in this chapter.

4.1. Power Requirements

The power is connected through the PC/104 power connector; or the separate power connector on the board. The supply uses only +5Volts and a ground connection.

Attention!
Be sure the power plug is wired correctly before supplying power to the board! A built-in diode protects the board against reverse polarity.

Tolerance of the 5V supply: 5Volt ±5%; the power-fail signal starts at ±10% of the 5V norm and generates a reset status for the MICROSPACE PC.

Test environment for the power consumption measurement:

Peripheries:

- Hard disk Hitachi Mod-HTS424020M9AT00 20GB
- Monitor Eizo Flexscan F340i.W
- PS/2-KB Logitech Mod-iTouch Keyboard
- PS/2-MS Logitech Mod-M-CAA43
- Floppy TEAC Mod-FD-05HF

Software:

- MS-DOS V6.22
- WinXP

Current consumption @ 5Volt supply at -40°C/+25°C/+85°C:

Mode	**Memory**	**DLAG-Nr.**	**-30 °C**	**+25°C**	**+85 °C**
MSM800SEV-500MHz			[mA]	[mA]	[mA]
DOS: C:\	1GB			1600	
Win2000: Desktop	1GB			1600	

4.2. Boot Time

System Boot-Times:

Definitions/Boot-Medium	**Quick Boot**	**Normal Boot**
MSM800SEV-500MHz	time [s]	time [s]
From Hard disk-Hitachi Mod-DK233AA-60:		
Boot from Hard disk to “Starting MS-DOS”-Prompt	-	17
Boot from Hard disk to XP desktop	-	45
Booting without a storage device (only BIOS)		10

4.3. CPU, Boards and RAMs

4.3.1. CPUs of this MICROSPACE Product

Processor	Type	Clock
GEODE LX800	National	500MHz

4.3.2. Numeric Coprocessor

The numeric coprocessor is always integrated into the Pentium CPUs.

4.3.3. DDRAM Memory on MSM800SEV/SEL/BEV/BEL

Speed	333
Size	DDR-SODIMM
	DDRDIMM 200pin
Bits	64bit
Capacity	256-1024 MByte
	DDR-SODIMM
Bank	1

4.3.4. DDRAM Memory on MSM800XEV/XEL

Speed	333
Size	DDR-Chips (BGA)
Bits	64bit
Capacity	256MByte
Bank	1

4.4. Interfaces

4.4.1. AT Compatible Keyboard & PS/2 Mouse X31

Pin	Signal
Pin 1	Speaker out
Pin 2	GND
Pin 3	External reset input
Pin 4	VCC
Pin 5	Keyboard Data
Pin 6	Keyboard Clock
Pin 7	GND
Pin 8	NC
Pin 9	Mouse Clock (PS/2)
Pin 10	Mouse Data (PS/2)

4.4.2. Line Printer Port LPT1

A standard bi-directional LPT port is integrated into the MICROSPACE PC.

Further information about these signals is available in numerous publications, including the IBM technical reference manuals for the PC and AT computers and from other reference documents.

The current is: IOH = 12mA IOL = 24mA

4.4.3. Serial Ports COM1-COM2

The serial channels are fully compatible with 16C550 UARTS. COM1 is the primary serial port and is supported by the board's ROM-BIOS as the PC-DOS 'COM1' device. The secondary serial port is COM2; it is supported as the 'COM2' device.

Standard: COM 1/2: National PC87317VUL: 2 x 16C550 compatible serial interfaces

Serial Port Connectors COM1, COM2:

Pin	Signal Name	Function	in/out	DB25 Pin	DB9 Pin
1	CD	Data Carrier Detect	in	8	1
2	DSR	Data Set Ready	in	6	6
3	RXD	Receive Data	in	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear to Send	in	5	8
7	DTR	Data Terminal Ready	out	20	4
8	RI	Ring Indicator	in	22	9
9	GND	Signal Ground		7	5

The serial port signals are compatible with the RS232C specifications.

4.4.4. Floppy Disk Interface

The onboard floppy disk controller and ROM-BIOS support one or two floppy disk drives in any of the standard PC-DOS and MS-DOS formats shown in the table.

Supported Floppy Formats:

Capacity	Drive size	Tracks	Data rate	DOS version
1.2MB	5-1/4"	80	500KHz	3.0 - 6.22
720K	3-1/2"	80	250KHz	3.2 - 6.22
1.44M	3-1/2"	80	500KHz	3.3 - 6.22

Floppy Interface Configuration

The desired configuration of floppy drives (number and type) must be properly initialized in the board's CMOS - configuration memory. This is generally done by using DEL or F2 at boot up time.

Floppy Interface Connector

The table shows the pin-out and signal definitions of the board's floppy disk interface connector. It is identical in pin-out to the floppy connector of a standard AT. Note that, as in a standard PC or AT, both floppy drives are jumpered to the same drive select: as the 'second' drive. The drives are uniquely selected as a result of a swapping of a group of seven wires (conductors 10-16) that must be in the cable between the two drives. The seven-wire swap goes between the computer board and drive 'A'; the wires to drive 'B' are unswapped (or swapped a second time). The 26pin high density (1mm pitch FCC) connector has only one drive and motor select. The onboard jumper defines the drive A: or B:. Default is always A:.

Floppy Disk Interface Technology

Only CMOS drives are supported. This means the termination resistors are 1 KOhm and 5 1/4“-drives are not recommended (TTL interface).

The 26pin connector: FFC/FPC 0.3mm thick 1.0mm (0.039") pitch (MOLEX 52030 Series)

Floppy Disk Interface Connector:

FD26: Pin	Signal Name	Function	in/out
1	VCC	+5Volt	
2	IDX	Index Pulse	in
3	VCC	+5Volt	
4	DS2	Drive Select 2	out
5	VCC	+5Volt	
6	DCHG	Disk Change	in
10	M02	Motor On 2	out
12	DIRC	Direction Select	out
14	STEP	Step	out
16	WD	Write Data	out
17	GND	Signal grounds	
18	WE	Write Enable	out
19	GND	Signal grounds	
20	TRKO	Track 0	in
21	GND	Signal grounds	
22	WP	Write Protect	in
23	GND	Signal grounds	
24	RDD	Read Data	in
25	GND	Signal grounds	
26	HS	Head Select	out

4.4.5. Speaker Interface

One of the board's CPU devices provides the logic for a PC compatible speaker port. The speaker logic signal is buffered by a transistor amplifier, and provides approximately 0.1Watt of audio power to an external 8 ohm speaker. Connect the speaker between VCC and speaker output to have no quiescent current.

4.5. Controllers

4.5.1. Interrupt Controllers

An 8259A compatible interrupt controller, within the chipset, provides seven prioritized interrupt levels. Of these, several are normally associated with the board's onboard device interfaces and controllers, and several are available on the AT expansion bus.

Interrupt	Sources	Onboard use
IRQ0	ROM-BIOS clock tick function, from timer 0	yes
IRQ1	Keyboard controller output buffer full	yes
IRQ2	Used for cascade 2. 8259	yes
IRQ3	COM2 serial port	yes
IRQ4	COM1 serial port	yes
IRQ5	LPT2 parallel printer (if present)	no *
IRQ6	Floppy controller	yes
IRQ7	LPT1 parallel printer	yes
IRQ8	Battery backed clock	yes
IRQ9	Free for user	no *
IRQ10	Free for user	no *
IRQ11	Free for user	no *
IRQ12	PS/2 mouse	yes
IRQ13	Math. coprocessor	yes
IRQ14	Hard disk IDE	yes
IRQ15	Free for user	no *

* May depend on the LAN configuration

4.6. Timers and Counters

4.6.1. Programmable Timers

An 8253 compatible timer/counter device is also included in the board's ASIC device. This device is utilized in precisely the same manner as in a standard AT implementation. Each channel of the 8253 is driven by a 1.190MHz clock, derived from a 14.318MHz oscillator, which can be internally divided in order to provide a variety of frequencies.

Timer 2 can also be used as a general purpose timer if the speaker function is not required.

Timer Assignment:

Timer	Function
0	ROM-BIOS clock tick (18.2Hz)
1	DRAM refresh request timing (15µs)
2	Speaker tone generation time base

4.6.2. RTC (Real Time Clock)

An AT compatible date/time clock is located within the chipset. The device also contains a CMOS static RAM, compatible with that in standard ATs. System configuration data is normally stored in the clock chip's CMOS RAM in a manner consistent with the convention used in other AT compatible computers.

Connect an external Lithium battery to X33 pin6 (or use the mounted battery). ***Be sure to use the correct polarity!***

The battery-backed clock can be set by using the DIGITAL-LOGIC AG SETUP at boot-time.

Note…
On all MSM800SEL/BEL/XEL boards – the battery must be connected externally! There is no battery assembled onboard.

Attention!
For systems that already have an onboard battery (MSM800SEV/BEV/XEV): if an external battery is to be connected, then the onboard battery **must** be removed first.

4.6.3. Watchdog

The watchdog timer detects a system crash and performs a hardware reset. After power up, the watchdog is always disabled as the BIOS does not send strobes to the watchdog. In case the user wants to take advantage of the watchdog, the application must produce a strobe at least every 800 ms. If no strobe occurs within the 800 ms, the watchdog resets the system.

For more information, please refer to the driver/software/BIOS manual “GEODE_LX800” on the Product CD. The watchdog feature is integrated in the INT15 function.

There are some programming examples available:
 Product CD-Rom or customer download area: \tools\SM855\int15dl\…

4.7. BIOS

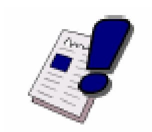
4.7.1. Core BIOS download

4.7.1.1. Before downloading a BIOS

Please read through this section carefully and prepare for the download.

Make a bootable diskette which includes the following files:

Flashrom.com
core BIOS xxxxxxxx.yyy



Important...
Do not use boot disks created in a Windows operating system. If you do not have an MSDOS 6.22 disk available, you can download a boot disk from www.bootdisk.com.

NOTE:

- Select the SHADOW option in the BIOS, for a BIOS and VGA (if this option is available).
- Disable the EMM386 or other memory managers in the CONFIG.SYS of your boot disk.
- Make sure that the Flashrom.com program and the BIOS to download are on the same path and directory!
- Boot the DOS without config.sys and autoexec.bat → press **F5** while starting the DOS boot.
- Check, where the Flashrom.com is located, that the available disk space is larger than 64kB (for safe storage).
- Make sure the floppy disk is not write-protected.

4.7.1.2. Start the download

1. Start the system with the bootable diskette. If you do not have a bootable diskette or floppy drive, you can start in DOS mode by pressing the **F5** key to disable autoexec.bat and config.sys.

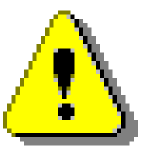
2. Run Flashrom.com.
   (In some cases you have to try the following: FLASHROM /D /sFFFC0000 biosname.xxx)

3. Power off the system.
   After powering on the system, press **F1** to enter setup and set the default values; then "save and leave" the setup.

4. Switch off the system after the download is finished.

4.7.1.3. If the download does not work:

- Check, if the EMM386 is not loaded.
- Check if there is a peripheral card in the system, which would occupy the same memory range. If one is present, disconnect it.
- If the download stopped or did not finish, make a warm boot* and repeat the steps or download another file. (* As the video is shadowed, everything is visible and a cold boot would clear the screen so nothing would be visible afterwards.)



Attention!
NEVER UPDATE A BIOS WITH A USB MEMORY STICK!!
THE SYSTEM WILL CRASH DURING THE DOWNLOAD!
Only use a USB or a standard floppy

Also, if you have two IDE devices attached to the board (e.g. HDD and CD-ROM), disconnect the CD-ROM before downloading the BIOS.

4.7.2. ROM-BIOS Sockets

An EPROM socket with 8bit wide data access normally contains the board's AT compatible ROM-BIOS. The socket takes a 29F020 EPROM (or equivalent) device. The board's wait-state control logic automatically inserts four memory wait states in all CPU accesses to this socket. The ROM-BIOS sockets occupy the memory area from C0000H through FFFFFh; however, the board's ASIC logic reserves the entire area from C0000h through FFFFFh for onboard devices, so that this area is already usable for ROM-DOS and BIOS expansion modules. Consult the appropriate address map for the MICROSPACE PC-Product ROM-BIOS sockets.

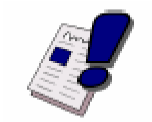
4.7.2.1. Standard BIOS ROM

Device:	FWH	
Map:	E0000 - FFFFFh	Core BIOS 128k
	C0000 - C7FFFh	VGA BIOS 32k
	CC000 - CFFFFh	FREE

4.7.3. BIOS CMOS Setup

If wrong setups are memorized in the CMOS-RAM, the default values will be loaded after resetting the RTC/CMOS-RAM by de-soldering the battery.

If the battery is down, it is always possible to start the system with the default values from the BIOS.



Note...
For the MSM800BEV/XEV/XEL: Should the product have an inaccurate BIOS setup and won't boot up, proceed as follows. (The installed BIOS must be V1.20 or newer.)

1. Set J7
2. Turn the power on
3. Press F1 to enter the BIOS setup
4. Select "L" to load the BIOS default settings
5. Remove J7
6. Select "X" to save and exit the BIOS setup

4.8. CMOS RAM Map

Systems based on the industry-standard specification include a battery backed Real Time Clock chip. This clock contains at least 64Bytes of non-volatile RAM. The system BIOS uses this area to store information including system configuration and initialization parameters, system diagnostics, and the time and date. This information remains intact even when the system is powered down.

The BIOS supports 128Bytes of CMOS RAM. This information is accessible through I/O ports 70h and 71h. CMOS RAM can be divided into several segments:

- Locations 00h - 0Fh contain the real time clock (RTC) and status information
- Locations 10h - 2Fh contain system configuration data
- Locations 30h - 3Fh contain system BIOS-specific configuration data as well as chipset-specific information
- Locations 40h - 7Fh contain chipset-specific information as well as power management configuration parameters

The following table provides a summary of how these areas may be further divided.

Beginning	Ending	Checksum	Description
00h	0Fh	No	RTC and Checksum
10h	2Dh	Yes	System Configuration
2Eh	2Fh	No	Checksum Value of 10h - 2Dh
30h	33h	No	Standard CMOS
34h	3Fh	No	Standard CMOS - SystemSoft Reserved
40h	5Bh	Yes	Extended CMOS - Chipset Specific
5Ch	5Dh	No	Checksum Value of 40h - 5Bh
5Eh	6Eh	No	Extended CMOS - Chipset Specific
6Fh	7Dh	Yes	Extended CMOS - Power Management
7Eh	7Fh	No	Checksum Value of 6Fh - 7Dh

CMOS Map

Location	Description
00h	Time of day (seconds) specified in BCD
01h	Alarm (seconds) specified in BCD
02h	Time of day (minutes) specified in BCD
03h	Alarm (minutes) specified in BCD
04h	Time of day (hours) specified in BCD
05h	Alarm (hours) specified in BCD
06h	Day of week specified in BCD
07h	Day of month specified in BCD
08h	Month specified in BCD
09h	Year specified in BCD
0Ah	Status Register A Bit 7 = Update in progress Bits 6-4 = Time based frequency divider Bits 3-0 = Rate selection bits that define the periodic interrupt rate and output frequency.
0Bh	Status Register B Bit 7 = Run/Halt 0 Run 1 Halt Bit 6 = Periodic Timer 0 Disable 1 Enable Bit 5 = Alarm Interrupt 0 Disable 1 Enable Bit 4 = Update Ended Interrupt 0 Disable 1 Enable Bit 3 = Square Wave Interrupt 0 Disable 1 Enable Bit 2 = Calendar Format 0 BCD 1 Binary Bit 1 = Time Format 0 12-Hour 1 24-Hour Bit 0 = Daylight Savings Time 0 Disable 1 Enable

Continued...

CMOS Map *continued...*

Location	Description
0Ch	Status Register C Bit 7 = Interrupt Flag Bit 6 = Periodic Interrupt Flag Bit 5 = Alarm Interrupt Flag Bit 4 = Update Interrupt Flag Bits 3-0 = Reserved
0Dh	Status Register D Bit 7 = Real Time Clock 0 Lost Power 1 Power
0Eh	CMOS Location for Bad CMOS and Checksum Flags Bit 7 = Flag for CMOS Lost Power 0 = Power OK 1 = Lost Power Bit 6 = Flag for CMOS checksum bad 0 = Checksum is valid 1 = Checksum is bad
0Fh	Shutdown Code
10h	Diskette Drives Bits 7-4 = Diskette Drive A 0000 = Not installed 0001 = Drive A = 360 kB 0010 = Drive A = 1.2MB 0011 = Drive A = 720 kB 0100 = Drive A = 1.44MB 0101 = Drive A = 2.88MB Bits 3-0 = Diskette Drive B 0000 = Not installed 0001 = Drive B = 360 kB 0010 = Drive B = 1.2MB 0011 = Drive B = 720 kB 0100 = Drive B = 1.44MB 0101 = Drive B = 2.88MB
11h	Reserved
12h	Fixed (Hard) Drives Bits 7-4 = Hard Drive 0, AT Type 0000 = Not installed 0001-1110 = Types 1-14 1111 = Extended drive types 16-44. See location 19h. Bits 3-0 = Hard Drive 1, AT Type 0000 = Not installed 0001-1110 = Types 1-14 1111 = Extended drive types 16-44. See location 2Ah.
13h	Reserved

Continued...

CMOS Map *continued...*

Location	Description
14h	Equipment Bits 7-6 = Number of Diskette Drives 00 = One diskette drive 01 = Two diskette drives 10, 11 = Reserved Bits 5-4 = Primary Display Type 00 = Adapter with option ROM 01 = CGA in 40 column mode 10 = CGA in 80 column mode 11 = Monochrome Bits 3-2 = Reserved Bit 1 = Math Coprocessor Presence 0 = Not installed 1 = Installed Bit 0 = Bootable Diskette Drive 0 = Not installed 1 = Installed
15h	Base Memory Size (in kB) - Low Byte
16h	Base Memory Size (in kB) - High Byte
17h	Extended Memory Size (in kB) - Low Byte
18h	Extended Memory Size (in kB) - High Byte
19h	Extended Drive Type - Hard Drive 0
1Ah	Extended Drive Type - Hard Drive 1
1Bh	Custom and Fixed (Hard) Drive Flags Bits 7-6 = Reserved Bit 5 = Internal Floppy Disk Controller 0 = Disabled 1 = Enabled Bit 4 = Internal IDE Controller 0 = Disabled 1 = Enabled Bit 3 = Hard Drive 0 Custom Flag 0 = Disabled 1 = Enabled Bit 2 = Hard Drive 0 IDE Flag 0 = Disabled 1 = Enabled Bit 1 = Hard Drive 1 Custom Flag 0 = Disabled 1 = Enabled Bit 0 = Hard Drive 1 IDE Flag 0 = Disabled 1 = Enabled
1Ch	Reserved
1Dh	EMS Memory Size Low Byte
1Eh	EMS Memory Size High Byte
1Fh - 24h	Custom Drive Table 0 These 6 Bytes (48 bits) contain the following data: Cylinders 10bits range 0-1023 Landing Zone 10bits range 0-1023 Write Precompensation 10bits range 0-1023 Heads 8bits range 0-15 Sectors/Track 8bits range 0-254

Continued...

CMOS Map *continued...*

Location	Description
1Fh	Byte 0 Bits 7-0 = Lower 8 bits of Cylinders
20h	Byte 1 Bits 7-2 = Lower 6 bits of Landing Zone Bits 1-0 = Upper 2 bits of Cylinders
21h	Byte 2 Bits 7-4 = Lower 4 bits of Write Precompensation Bits 3-0 = Upper 4 bits of Landing Zone
22h	Byte 3 Bits 7-6 = Reserved Bits 5-0 = Upper 6 bits of Write Precompensation
23h	Byte 4 Bits 7-0 = Number of Heads
24h	Byte 5 Bits 7-0 = Sectors Per Track
25h - 2Ah	Custom Drive Table 1 These 6 Bytes (48 bits) contain the following data: Cylinders 10bits range 0-1023 Landing Zone 10bits range 0-1023 Write Precompensation 10bits range 0-1023 Heads 8bits range 0-15 Sectors/Track 8bits range 0-254
25h	Byte 0 Bits 7-0 = Lower 8 bits of Cylinders
26h	Byte 1 Bits 7-2 = Lower 6 bits of Landing Zone Bits 1-0 = Upper 2 bits of Cylinders
27h	Byte 2 Bits 7-4 = Lower 4 bits of Write Precompensation Bits 3-0 = Upper 4 bits of Landing Zone
28h	Byte 3 Bits 7-6 = Reserved Bits 5-0 = Upper 6 bits of Write Precompensation
29h	Byte 4 Bits 7-0 = Number of Heads
2Ah	Byte 5 Bits 7-0 = Sectors Per Track
2Bh	Boot Password Bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password Bits 6-0 = Calculated Password
2Ch	SCU Password Bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password Bits 6-0 = Calculated Password

Continued...

CMOS Map *continued...*

Location	Description
2Dh	Reserved
2Eh	High Byte of Checksum - Locations 10h to 2Dh
2Fh	Low Byte of Checksum - Locations 10h to 2Dh
30h	Extended RAM (kB) detected by POST - Low Byte
31h	Extended RAM (kB) detected by POST - High Byte
32h	BCD Value for Century
33h	Base Memory Installed Bit 7 = Flag for Memory Size 0 = 640kB 1 = 512kB Bits 6-0 = Reserved
34h	Minor CPU Revision Differentiates CPUs within a CPU type (i.e., 486SX vs 486 DX, vs 486 DX/2). This is crucial for correctly determining CPU input clock frequency. During a power-on reset, Reg DL holds minor CPU revision.
35h	Major CPU Revision Differentiates between different CPUs (i.e., 386, 486, Pentium). This is crucial for correctly determining CPU input clock frequency. During a power-on reset, Reg DH holds major CPU revision.
36h	Hotkey Usage Bits 7-6 = Reserved Bit 5 = Semaphore for Completed POST Bit 4 = Semaphore for 0 Volt POST (not currently used) Bit 3 = Semaphore for already in SCU menu Bit 2 = Semaphore for already in PM menu Bit 1 = Semaphore for SCU menu call pending Bit 0 = Semaphore for PM menu call pending
40h-7Fh	Definitions for these locations vary depending on the chipset.

4.9. EEPROM saved CMOS Setup

The EEPROM has different functions, as listed below:

- Backup of the CMOS-Setup values.
- Storing system information (i.e., version, production date, customization of the board, CPU type).
- Storing user/application values.

The EEPROM will be updated automatically after exiting the BIOS setup menu. The system will operate also without any CMOS battery. While booting, the CMOS is automatically updated with the EEPROM values.

Press the Esc-key while powering on the system before the video shows the BIOS message and the CMOS will **not** be updated.

This would be helpful, if wrong parameters are stored in the EEPROM and the setup of the BIOS does not start.

If the system hangs or a problem appears, the following steps must be performed:

1. Reset the CMOS-Setup (disconnect the battery for at least 10 minutes).
2. Press **Esc** until the system starts up.
3. Enter the BIOS Setup:
    a. load DEFAULT values
    b. enter the settings for the environment
    c. exit the setup
4. Restart the system.

The user may access the EEPROM through the INT15 special functions. Refer to that chapter in the GEODE LX800 manual on the Product CD.

The system information is read-only and uses the SFI functions. Refer to the GEODE LX800 manual.

4.9.1. EEPROM Memory for Setup

The EEPROM is used for setup and configuration data, stored as an alternative to the CMOS-RTC. Optionally, the EEPROM setup driver may update the CMOS RTC, if the battery is running down and the checksum error would appear and stop the system. The capacity of the EEPROM is 2 kByte.

Organization of the 2048Byte EEPROMs:

Address MAP:	Function:
0000h	**CMOS-Setup valid (01=valid)**
0001h	**Reserved**
0003h	**Flag for DLAG-Message (FF=no message)**
0010h-007Fh	**Copy of CMOS-Setup data**
0080h-00FFh	**Reserved for AUX-CMOS-Setup**
0100h-010Fh	**Serial-Number**
0110h-0113h	Production date (year/day/month)
0114h-0117h	1. Service date (year/day/month)
0118h-011Bh	2. Service date (year/day/month)
011Ch-011Fh	3. Service date (year/day/month)
0120h-0122h	Boot errors (Auto incremented if any boot error occurs)
0123h-0125h	Setup Entries (Auto incremented on every Setup entry)
0126h-0128h	Low Battery (Auto incremented every time the battery is low, EEPROM -> CMOS)
0129h-012Bh	Startup (Auto incremented on every power-on start)
0130h	Reserved
0131h	Reserved
0132h/0133h	BIOS Version (V1.4 => [0132h]:= 4, [0133h]:=1)
0134h/0135h	BOARD Version (V1.5 => [0124h]:=5, [0125h]:=1)
0136h	BOARD TYPE (‘M’=PC/104, ‘E’=Euro, ‘W’=MSWS, ‘S’=Slot, ‘C’=Custom, ‘X’= smartCore or smartModule)
0137h	CPU TYPE: (01h=ELAN300/310, 02h=ELAN400, 05h=P5, 08h=P3, 09h=ELAN520, 10h=P-M).
0200h-03FFh	**Reserved**
0200h-027Fh	Reserved
0400h-07FFh	**Free for Customer use**

4.10. Memory & I/O Map

4.10.1. System Memory Map

The X86 CPU, used as a central processing unit on the MICROSPACE, has a memory address space which is defined by 32 address bits. Therefore, it can address 1 GByte of memory. The memory address MAP is as follows:

CPU GEODE

Address:	Size:	Function / Comments:
000000 - 09FFFFh	640kBytes	Onboard DRAM for DOS applications
0A0000 - 0BFFFFh	128kBytes	CGA, EGA, LCD Video RAM 128kB
0C0000 - 0C7FFFh 0C8000 - 0CFFFFh	32kBytes 32kBytes	VGA BIOS Free for user
0D0000 - 0DFFFFh	64kBytes	Free for user
0E0000 - 0EBFFFh 0EC000 - 0EFFFFh	32kBytes 16kBytes	Bios BIOS extensions
0F0000 - 0FFFFFh	64kBytes	Core BIOS
100000 - 1FFFFFFh	31MBytes	DRAM for extended onboard memory

4.10.2. System I/O Map

The following table details the legacy I/O range for 000h through 4FFh. Each I/O location has a read/write (R/W) capability.

Note the following abbreviations:

---	Unknown or cannot be determined.
Yes	Read and write the register at the indicated location. No shadow required.
WO	Write only. Value written can not be read back. Reads do not contain any useful information.
RO	Read only. Writes have no effect.
Shw	The value written to the register can not be read back via the same I/O location. Read back is accomplished via a "Shadow" register located in MSR space.
Shw@	Reads of the location return a constant or meaningless value.
Shw$	Reads of the location return a status or some other meaningful information.
Rec	Writes to the location are "recorded" and written to the LPC. Reads to the location return the recorded value. The LPC is not read.

I/O Map

I/O Addr.	Function	Size	R/W	Comment
000h	Slave DMA Address - Channel 0	8bit	Yes	16bit values in two transfers.
001h	Slave DMA Counter - Channel 0	8bit	Yes	16bit values in two transfers.
002h	Slave DMA Address - Channel 1	8bit	Yes	16bit values in two transfers.
003h	Slave DMA Counter - Channel 1	8bit	Yes	16bit values in two transfers.
004h	Slave DMA Address - Channel 2	8bit	Yes	16bit values in two transfers.
005h	Slave DMA Counter - Channel 2	8bit	Yes	16bit values in two transfers.
006h	Slave DMA Address - Channel 3	8bit	Yes	16bit values in two transfers.
007h	Slave DMA Counter - Channel 3	8bit	Yes	16bit values in two transfers.
008h	Slave DMA Command/Status - Channels [3:0]	8bit	Shw$	
009h	Slave DMA Request - Channels [3:0]	8bit	WO	Reads return value B2h.
00Ah	Slave DMA Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Bh	Slave DMA Mode - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Ch	Slave DMA Clear Pointer - Channels [3:0]	8bit	WO	Reads return value B2h.
00Dh	Slave DMA Reset - Channels [3:0]	8bit	WO	Reads return value B2h.
00Eh	Slave DMA Reset Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Fh	Slave DMA General Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
010h-01Fh	No Specific Usage	---	---	
020h	PIC Master - Command/Status	8bit	Shw$	
021h	PIC Master - Command/Status	8bit	Shw$	
022h-03Fh	No Specific Usage	---	---	
040h	PIT – System Timer	8bit	Shw$	
041h	PIT – Refresh Timer	8bit	Shw$	
042h	PIT – Speaker Timer	8bit	Shw$	
043h	PIT – Control	8bit	Shw$	
044h-05Fh	No Specific Usage	---	---	

Continued…

I/O Map *Continued…*

I/O Addr.	Function	Size	R/W	Comment
060h	Keyboard/Mouse - Data Port	8bit	Yes	If KEL Memory Offset 100h[0] = 1(Emulation-Enabled bit). If MSR 5140001Fh[0] = 1 (SNOOP bit) and KEL Memory Offset 100h[0] = 0 (Emulation-Enabled bit).
061h	Port B Control	8bit	Yes	
062h-063h	No Specific Usage	---	---	
064h	Keyboard/Mouse - Command/ Status	8bit	Yes	If KEL Memory Offset 100h[0] = 1 (Emulation-Enabled bit). . If MSR 5140001Fh[0] = 1 (SNOOP bit) and KEL Memory Offset 100h[0] = 0 (Emulation-Enabled bit)
065h-06Fh	No Specific Usage	---	---	
070h-071h	RTC RAM Address/Data Port	8bit	Yes	Options per MSR 51400014h[0]. (***Note 1***)
072h-073h	High RTC RAM Address/Data Port	8bit	Yes	Options per MSR 51400014h[1].
074-077h	No Specific Usage	---	---	
078h-07Fh	No Specific Usage	---	---	
080h	Post Code Display	8bit	Rec	Write LPC and DMA. Read only DMA.
081h	DMA Channel 2 Low Page			
082h	DMA Channel 3 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
083h	DMA Channel 1 Low Page			
084h-086h	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only DMA.
087h	DMA Channel 0 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
088h	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only DMA.
089h	DMA Channel 6 Low Page			
08Ah	DMA Channel 7 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
08B	DMA Channel 5 Low Page			
08Ch-08Dh	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only
08Eh	DMA			
08Fh	DMA C4 Low Page	8bit	Rec	Upper addr bits [23:16]. See comment at 080h.
090h-091h	No Specific Usage	---	---	
092h	Port A	8bit	Yes	If kel_porta_en is enabled, then access Port A; else access LPC.
093h-09Fh	No Specific Usage	---	---	
0A0h	PIC Slave - Command/Status	8bit	Shw$	
0A1h	PIC Slave - Command/Status	8bit	Shw$	
0A2h-0BFh	No Specific Usage	8bit	---	
0C0h	Master DMA Address - Channel 4	8bit	Yes	16bit values in two transfers.
0C1h	No Specific Usage	8bit	---	
0C2h	Master DMA Counter - Channel 4	8bit	Yes	16bit values in two transfers.
0C3h	No Specific Usage	8bit	---	
0C4h	Master DMA Address - Channel 5	8bit	Yes	16bit values in two transfers.
0C6h	Master DMA Counter - Channel 5	8bit	Yes	16bit values in two transfers.
0C7h	No Specific Usage	8bit	---	
0C8h	Master DMA Address - Channel 6	8bit	Yes	16bit values in two transfers.
0CAh	Master DMA Counter - Channel 6	8bit	Yes	16bit values in two transfers.
0CBh	No Specific Usage	8bit	---	

Continued…

I/O Map *Continued…*

I/O Addr.	Function	Size	R/W	Comment
0CCh	Master DMA Address - Channel 7	8bit	Yes	16bit values in two transfers.
0CDh	No Specific Usage	8bit	---	
0CEh	Master DMA Counter - Channel 7	8bit	Yes	16bit values in two transfers.
0CFh	No Specific Usage	8bit	---	
0D0h	Master DMA Command/Status – Channels [7:4]	8bit	Shw$	
0D1h	No Specific Usage	8bit	---	
0D2h	Master DMA Request - Channels [7:4]	8bit	WO	
0D3h	No Specific Usage	8bit	---	
0D4h	Master DMA Mask - Channels [7:4]	8bit	Yes	
0D5h	No Specific Usage	8bit	---	
0D6h	Master DMA Mode - Channels [7:4]	8bit	Shw@	
0D7h	No Specific Usage	8bit	---	
0D8h	Master DMA Clear Pointer - Channels [7:4]	8bit	WO	
0D9h	No Specific Usage	8bit	---	
0DAh	Master DMA Reset - Channels [7:4]	8bit	WO	
0DBh	No Specific Usage	8bit	---	
0DCh	Master DMA Reset Mask - Channels [7:4]	8bit	WO	
0DDh	No Specific Usage	8bit	---	
0DEh	Master DMA General Mask - Channels [7:4]	8bit	Shw@	
0DFh	No Specific Usage	8bit	---	
0E0h-2E7h	No Specific Usage	---	---	
2E8h-2EFh	UART/IR - COM4	8bit	---	MSR bit enables/disables into I/O 2EFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
2F0h-2F7h	No Specific Usage	---	---	
2F8h-2FFh	UART/IR - COM2	8bit	---	MSR bit enables/disables into I/O 2FFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
300h- 36Fh	No Specific Usage	---	---	
370h	Floppy Status R A	8bit	RO	Second Floppy.
371h	Floppy Status R B	8bit	RO	Second Floppy.
372h	Floppy Digital Out	8bit	Shw@	Second Floppy.
373h	No Specific Usage	8bit	---	
374h	Floppy Cntrl Status	8bit	RO	Second Floppy.
375h	Floppy Data	8bit	Yes	Second Floppy.
376h	No Specific Usage	8bit	---	
377h	Floppy Conf Reg	8bit	Shw$	Second Floppy.
378h-3E7h	No Specific Usage	---	---	
3E8h-3EFh	UART/IR - COM3	8bit	---	MSR bit enables/disables into I/O 3EFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
3F0h	Floppy Status R A	8bit	RO	First Floppy.

Continued…

I/O Map *Continued…*

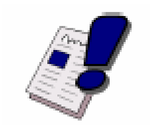
I/O Addr.	Function	Size	R/W	Comment
3F1h	Floppy Status R B	8bit	RO	First Floppy.
3F2h	Floppy Digital Out	8bit	Shw@	First Floppy.
3F3h	No Specific Usage	8bit	---	
3F4h	Floppy Cntrl Status	8bit	RO	First Floppy.
3F5h	Floppy Data	8bit	Yes	First Floppy.
3F6h	No Specific Usage	8bit	---	
3F7h	Floppy Conf Reg	8bit	Shw$	First Floppy.
3F8h-3FFh	UART/IR - COM1	8bit	---	MSR bit enables/disables into I/O 3FFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
480h	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
481h	DMA Channel 2 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
482h	DMA Channel 3 High Page			
483h	DMA Channel 1 High Page			
484h-486h	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
487h	DMA Channel 0 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
489h	DMA Channel 6 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
48Ah	DMA Channel 7 High Page			
48Bh	DMA Channel 5 High Page			
48Ch-48Eh	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
48Fh	DMA Channel 4 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
490h-4CFh	No Specific Usage	---	---	
4D0h	PIC Level/Edge	8bit	Yes	IRQ0-IRQ 7.
4D1h	PIC Level/Edge	8bit	Yes	IRQ8-IRQ15.
4D2h-4FFh	No Specific Usage	---	---	

Note 1: The Diverse Device Snoops writes to this port and maintains the MSB as NMI enabled. When low, NMI is enabled. When high, NMI is disabled. This bit defaults high. Reads of this port return bits [6:0] from the on-chip or off-chip target, while Bit 7 is returned from the “maintained” value.

5. VGA/LCD

5.1. VGA/LCD Controller of the Geode LX800

- Highly integrated flat panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, Clock Synthesizer, and integrated frame buffer
- HiQColorTM Technology implemented with TMED (Temporal Modulated Energy Distribution)
- Hardware Windows Acceleration
- Hardware Multimedia Support
- High-Performance flat panel display resolution and color depth at 3.3V
- 18/24bit direct interface to color TFT panels (X1)
- Advanced Power Management minimizes power usage in:
- Normal operation
- Standby (Sleep) modes
- Panel-Off Power-Saving Mode
- VESA standards supported
- Fully compatible with IBM® VGA
- Driver support for Windows XP, Windows 2000, Windows 98, Windows NT4.0



Note...
On the MSM800SEV/SEL, if the LCD ouput is used then the VGA/CRT output will not work.

5.2. Graphic Modes

Bios settings: 254MB video memory (shared)

Resolution	Col. Dept.	Frequency
800x600	16bit / 32bit	60Hz – 100Hz
1024x768	16bit / 32bit	60Hz – 100Hz
1152x864	16bit / 32bit	60Hz – 100Hz
1280x1024	16bit / 32bit	60Hz – 100Hz
1600x1200	16bit / 32bit	60Hz – 100Hz
1920x1440	16bit / 32bit	60Hz – 85Hz

5.3. DVICON Resolution

The maximum resoluton of the DVICON is 1600x1200.

5.4. Flat Panel Functional Description

The FP connects to the RGB port of the video mixer.

LCD Interface:

The FP interfaces directly to industry standard 18 or 24bit active matrix thin-film-transistor (TFT).

The digital RGB or video data that is supplied by the video logic is converted into a suitable format to drive a wide variety range of panels with variable bits.

The LCD interface includes dithering logic to increase the apparent number of colors displayed for use on panels with less than 6bits per color. The LCD interface also supports automatic power sequence off panel power supplies.

Mode Selection:

The FP can be configured for operation with most standard TFT panels in the bios setup:

- Supports TFT panels with 18 or 24bit interface with 320x240, 640x480, 800x600, 1024x768, 1280x1024, and 1600x1200 pixel resolutions. Either one or two pixels per clock is supported for all resolutions.
- For TFT panel support, the output from the dither block is directly fed onto the panel data pins (DRGBx). The data that is being sent onto the panel data pins is in sync with the TFT timing signals such as HSYNC, VSYNC, and LDE.
- One pixel (or two pixels in 2 pix/clk mode) is shifted on every positive edge of the clock as long as DISP_ENA is active.

Enter the BIOS with F1

- Select C (Motherboard Device Configuration)
- Select F (Video and Flat Panel Configuration
- Output Display = Flat Panel
  - Flat Panel Configuration
    - TYPE = TFT
      - Resolution = 320x240, 640x480, 800x600, 1024x768, 1280x1024, or 1600x1200 pixel

6. DESCRIPTION OF THE CONNECTORS

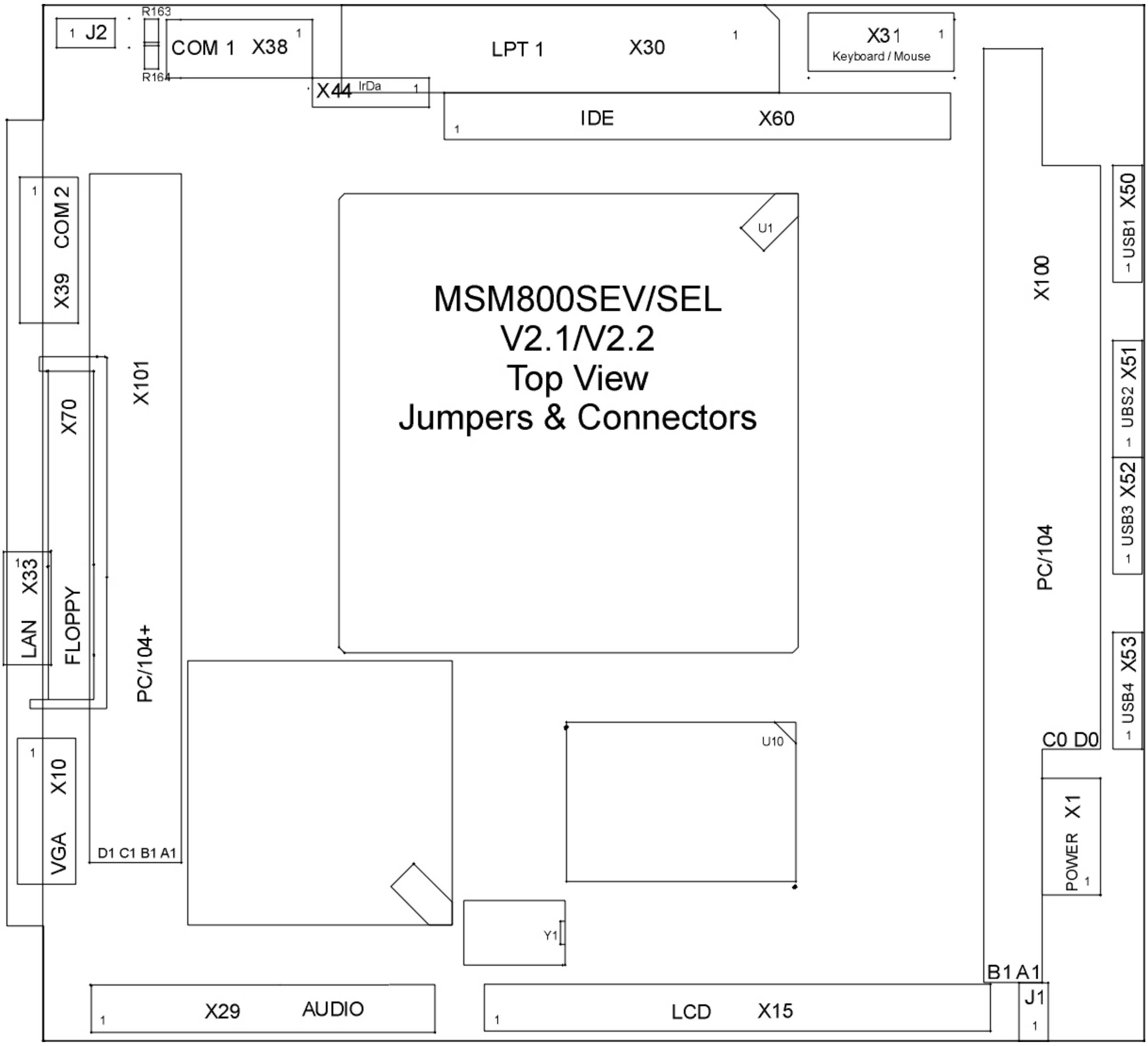
The following pages describe the connector pin-out for the MSM800SEV/SEL V2.1/V2.2, MSMBEV V1.1, and MSMXEV/XEL V1.0.

Flat cable

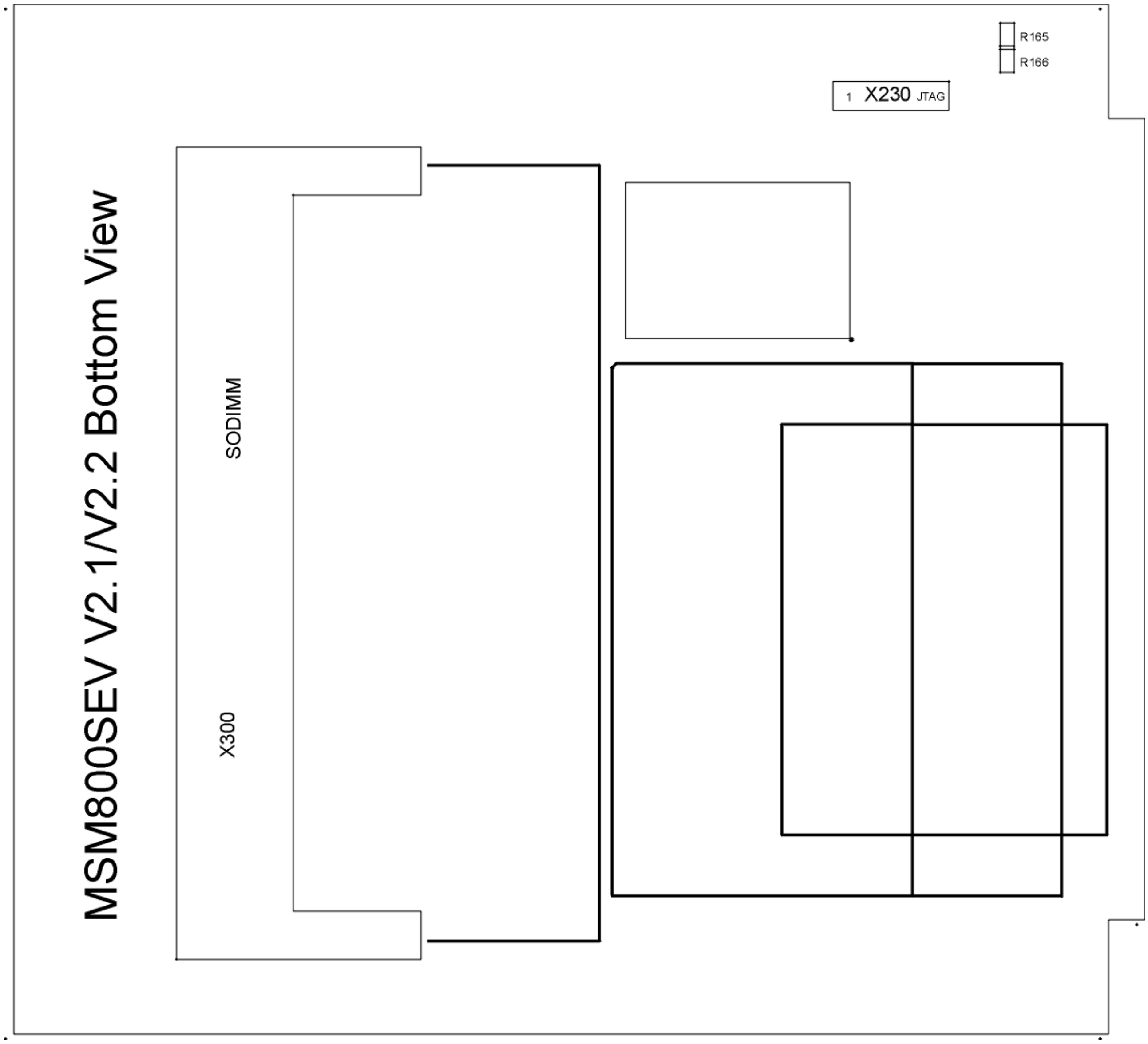
44pin IDE is:	IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable
All others are:	IDT Terminal for Dual Row 0.1" (2.54mm grid) and 1.27mm flat cable
NC:	not connected

Connector	Structure	Pin	Remarks
X1	Power	2x4	2.54mm
X10	VGA	2x5	2.54mm
X15	LCD	2x22	2mm
X29	Sound Audio I/O	2x15	2.00mm
X30	LPT1	2x13	2.54mm
X300	SODIMM	144	0.8mm
X31	Keyboard, mouse, utility	2x5	2.54mm
X33	LAN / Battery	2x5	2.00mm
X38	COM1	2x5	2.54mm
X39	COM2	2x5	2.54mm
X44	IrDA	4	2.54mm
X50	USB 1	4	2.54mm
X51	USB 2	4	2.54mm
X52	USB 3	4	2.54mm
X53	USB 4	4	2.54mm
X60	IDE	2x22	2mm
X70	Floppy	26	FCC micro
X71	CompactFlash Holder		
X100	PC104	104	2.54mm
X101	PC104+	120	2mm
X110	POD Port	2x7	2mm
X230	JTAG-Port	4	2.54mm

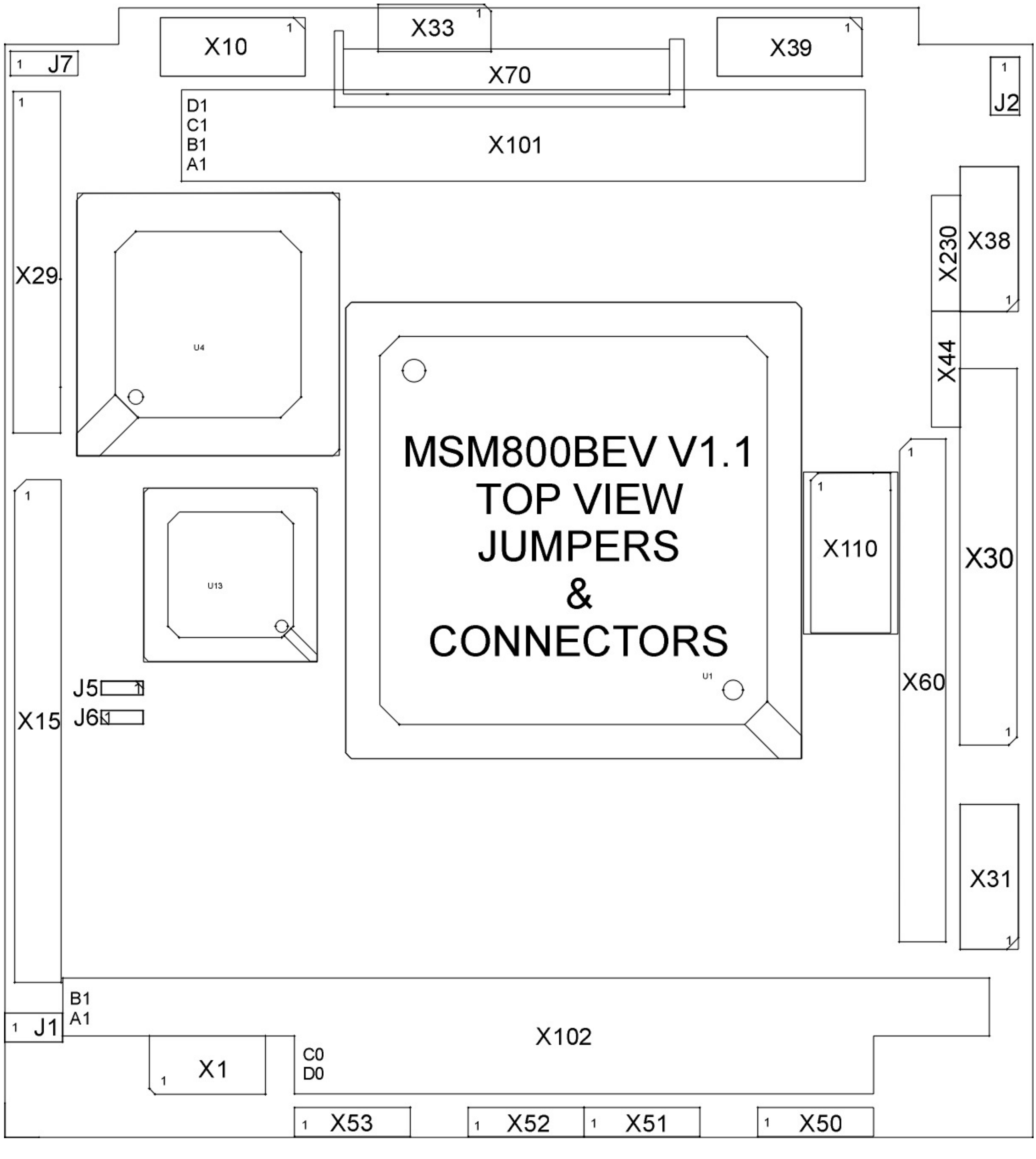
6.1. Top Side of the MSM800SEV/SEL V2.1/V2.2



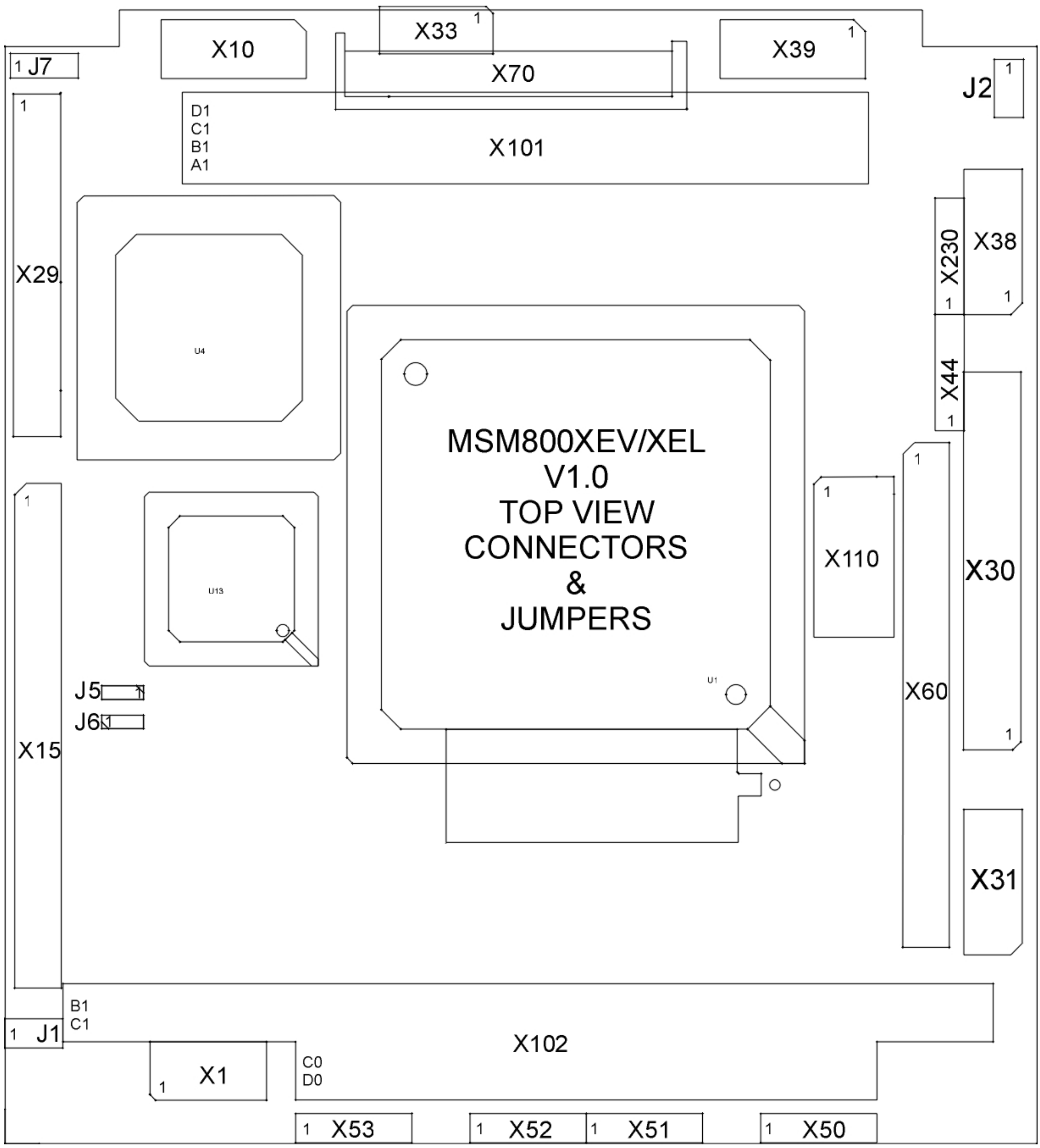
6.2. Bottom Side of the MSM800SEV V2.1/V2.2



6.3. Top Side of the MSM800BEV V1.1



6.4. Top Side of the MSM800XEV/XEL V1.0



X1 Power Supply

Pin	Signal	Pin	Signal
1	= GND	2	= VCCSUS +5Volt Input Supply
3	= NC	4	= (+12V input)
5	= NC	6	= Main_SW
7	= GND	8	= VCCSUS +5Volt Input Supply

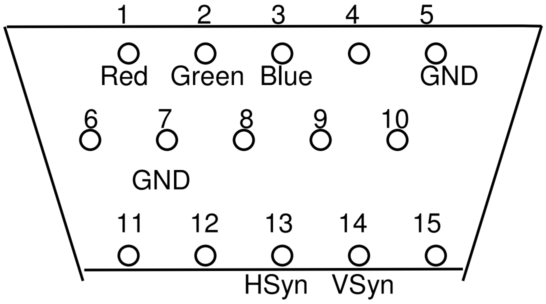
VCCSUS = 5Volt Main Supply Input

X10 VGA Monitor (CRT-signals)

J2 Header		15 pins HiDensity DSUB	
10 Pin -M	**Signal**	**Pin**	**Signal**
2	VGA red	1	Red
4	VGA green	2	Green
6	VGA blue	3	Blue
8	Horizontal Synch	13	H-Synch
9	Vertical Synch	14	V-Synch
		5 + 11	Bridged
1	Ground	5, 6, 7, 8	Ground
3	NC		
5	NC		
7	Serial_Data		
10	Serial_Clock		

The VGA-CRT signals from J2 must be wired to a standard VGA HiDensity DSub connector (female):
The LCD signals must be wired panel specific.

Solder-side view of the female 15pin HiDSub



X15 LCD TFT Interface (flat panel signals)

Pin	Signal	TFT 18bit	TFT 24bit
1	FPM (out)	LDE	LDE
2	CRT-Vert.Synch	VSYNC	VSYNC
3	Backlight Supply output (5/12V)*		
4	CRT-Horiz.Synch	HSYNC	HSYNC
5	VCC 3.3V		
6	Ground		
7	NC		
8	Shift Clock	CKL	CKL
9	VDD Supply output (3/5V)*	ENLVDD	ENLVDD
10	FP0		Blue 0
11	FP1		Blue 1
12	FP2	Blue 0	Blue 2
13	FP3	Blue 1	Blue 3
14	FP4	Blue 2	Blue 4
15	FP5	Blue 3	Blue 5
16	FP6	Blue 4	Blue 6
17	FP7	Blue 5	Blue 7
18	FP8		Green 0
19	FP9		Green 1
20	FP10	Green 0	Green 2
21	FP11	Green 1	Green 3
22	FP12	Green 2	Green 4
23	FP13	Green 3	Green 5
24	FP14	Green 4	Green 6
25	FP15	Green 5	Green 7
26	Ground		
27	FP16		Red 0
28	FP17		Red 1
29	FP18	Red 0	Red 2
30	FP19	Red 1	Red 3
31	FP20	Red 2	Red 4
32	FP21	Red 3	Red 5
33	FP22	Red 4	Red 6
34	FP23	Red 5	Red 7
35	NC		
36	Reserved PICR		
37	Reserved VPIC		
38	Reserved PIC_DAT		
39	Reserved PIC_CLK		
40	Reserved PIC_OSC1		
41	Ground		
42	NC		
43	+5Volt Supply (out)		
44	+12Volt Supply (out)		

* Since board version V2.1, the signals BKL (pin3) and VDD (pin9) can be used directly, without an external circuit

Pin	Signal Name	Supply		Supply jumper	Max. Current
3	BKL	5V	12V**	R165 / R166	1.5A
9	VDD	3.3V	5V	R163 / R164	1.5A

** The 12V will not generate on the board; you have to supply the 12V from an external PSU through the connector X1, pin4.

Please refer to the jumper list in Chapter 7 to install the supply jumpers correctly.

X29 Sound/Audio Port

Pin	Signal	Pin	Signal
1	Input_CD_L	2	GND
3	Input_CD_R	4	Input_AUX_L
5	GND	6	Input_AUX_R
7	Input_Line_L	8	GND
9	Input_Line_R	10	GND
11	Input_MIC 1	12	GND
13	Input_MIC 2	14	Input Mono
15	Output Front / Line Left	16	GND
17	Output Front / Line Right	18	GND
19	Output Surround Left	20	GND
21	Output Surround Right	22	GND
23	Output_Center	24	GND
25	Output_Subwoofer	26	GND
27	SPDIF Digital Output	28	Jack Sense 0 Input
29	Jack Sense 2 Input	30	Jack Sense 3 Input

The audio/sound feature is only available on the MSM800SEV board, **NOT** on the MSM800SEL.

X30 Printer Port (Centronics)

The printer connector provides an interface for 8bit Centronics printers.

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= Strobe
Pin 3	Pin 2	= Data 0
Pin 5	Pin 3	= Data 1
Pin 7	Pin 4	= Data 2
Pin 9	Pin 5	= Data 3
Pin 11	Pin 6	= Data 4
Pin 13	Pin 7	= Data 5
Pin 15	Pin 8	= Data 6
Pin 17	Pin 9	= Data 7
Pin 19	Pin 10	= Acknowledge
Pin 21	Pin 11	= Busy
Pin 23	Pin 12	= paper end
Pin 25	Pin 13	= select
Pin 2	Pin 14	= autofeed
Pin 4	Pin 15	= error
Pin 6	Pin 16	= init printer
Pin 8	Pin 17	= shift in (SI)
Pins 10, 12, 14, 16, 18, 26	Pin 18-22	= left open
Pins 20, 22, 24	Pin 23-25	= GND

X31 Keyboard PS/2/-Mouse Utility Connector

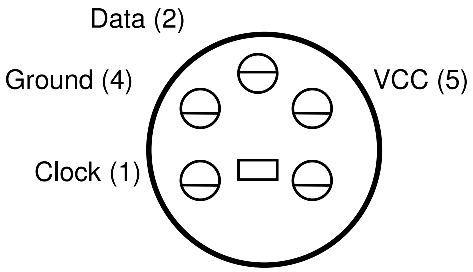
The speaker must be connected to VCC, to have a low, inactive current in the speaker.

Pin	Signal	Pin	Signal
1	= Speaker Out	2	= Ground (for Speaker)
3	= Reset In* (active low)	4	= VCC
5	= Keyboard Data	6	= Keyboard Clock
7	= Ground	8	= External Battery
9	= PS/2 Mouse Clock	10	= PS/2 Mouse Data

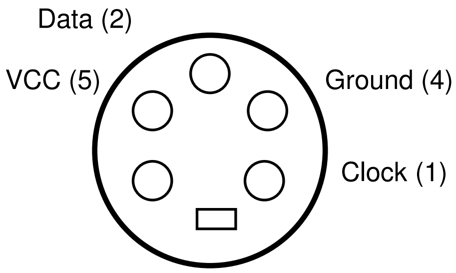
* Reset-In signal has an internal Pullup of 1k to 5Volt VCC.

The Utility connector must be wired to a standard AT-female connector:

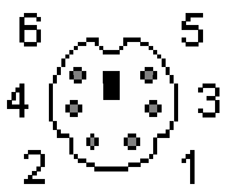
Front side AT-Keyboard (female)



Solder-side AT-Keyboard (female)



PS/2 Front side (female)



Connector and adapter

	Mini-DIN PS/2 (6 PC)	DIN 41524 (5 PC)	Remarks
Shield	Shield	Shield	KEYBOARD
DATA	1	2	
GND	3	4	
VCC (+5V)	4	5	
CLK	5	1	
	Mini-DIN PS/2 (6 PC)		
VCC (+5V)	4		MOUSE
DATA	1		
GND	3		
CLK	5		

X33 10/100 BASE-T Interface Connector

Pin *	Signal	Remarks
1	= TX-	Since board version V2.1, the LAN transformer is onboard
2	= TX+	
3	= RX-	
4	= RX+	
5	= Activity LED	
6	= BAT input 3.0-3.6V	Ext. Lithium battery (see also chapter 2.13.1)
7	= GND	
8	= VCC 3.3V	
9	= Speed LED	
10	= Link LED	

X38 Serial Port COM1

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= DCD
Pin 2	Pin 6	= DSR
Pin 3	Pin 2	= RxD
Pin 4	Pin 7	= RTS
Pin 5	Pin 3	= TxD
Pin 6	Pin 8	= CTS
Pin 7	Pin 4	= DTR
Pin 8	Pin 9	= RI
Pin 9	Pin 5	= GND
Pin 10		= NC

X39 Serial Port COM2

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= DCD
Pin 2	Pin 6	= DSR
Pin 3	Pin 2	= RxD
Pin 4	Pin 7	= RTS
Pin 5	Pin 3	= TxD
Pin 6	Pin 8	= CTS
Pin 7	Pin 4	= DTR
Pin 8	Pin 9	= RI
Pin 9	Pin 5	= GND
Pin 10		= NC

X44 IrDA Connector

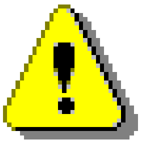
Pin	Signal
1	VCC
2	IRTX
3	IRRX
4	GND

BIOS settings:

You must enable the UART A of the GeodeLX in the BIOS setup:

F1→Mother board device configuration→I/O configuration:

- UART port A = enabled
- UART mode = SIR/CIR



Attention!

Never set the UART A mode to “Serial-16550 compatible” or “Extended” when an IrDA diode is connected to the X44 or **the diode will be destroyed!**

X50 USB 1 Connector

Pin	Signal
1	= VCC
2	= USB-P0-
3	= USB-P0+
4	= GND

X51 USB 2 Connector

Pin	Signal
1	= VCC
2	= USB-P0-
3	= USB-P0+
4	= GND

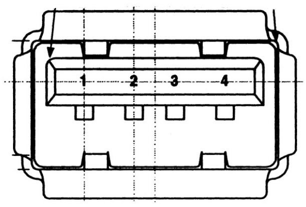
X52 USB 3 Connector

Pin	Signal
1	= VCC
2	= USB-P0-
3	= USB-P0+
4	= GND

X53 USB 4 Connector

Pin	Signal
1	= VCC
2	= USB-P0-
3	= USB-P0+
4	= GND

Pin 1	= VCC
Pin 2	= USB-P0-
Pin 3	= USB-P0+
Pin 4	= GND



X60 IDE Interface

Pin	Signal	Pin	Signal
1	= Reset (active low)	2	= GND
3	= D7	4	= D8
5	= D6	6	= D9
7	= D5	8	= D10
9	= D4	10	= D11
11	= D3	12	= D12
13	= D2	14	= D13
15	= D1	16	= D14
17	= D0	18	= D15
19	= GND	20	= (keypin) NC
21	= DREQ	22	= GND
23	= IOW (active low)	24	= GND
25	= IOR (active low)	26	= GND
27	= IORDY	28	= SPSYNC
29	= DACK	30	= GND
31	= IRQ14	32	= NC
33	= ADR1	34	= PDIAG
35	= ADR0	36	= ADR2
37	= CS0 (active low)	38	= CS1 (active low)
39	= LED (active low) asp	40	= GND
41	= VCC Logic	42	= VCC Motor
43	= GND	44	= NC

X70 Floppy Disk Interface Connector

FD26	Signal Name	Function	in/out
Pin 1	VCC	+5Volt	
Pin 2	IDX	Index Pulse	in
Pin 3	VCC	+5Volt	
Pin 4	DS2	Drive Select 2	out
Pin 5	VCC	+5Volt	
Pin 6	DCHG	Disk Change	in
Pin 7	NC		
Pin 8	NC		
Pin 9	NC		
Pin 10	M02	Motor On 2	out
Pin 11	NC		
Pin 12	DIRC	Direction Select	out
Pin 13	NC		
Pin 14	STEP	Step	out
Pin 15	GND		
Pin 16	WD	Write Data	out
Pin 17	GND	Signal grounds	
Pin 18	WE	Write Enable	out
Pin 19	GND	Signal grounds	
Pin 20	TRKO	Track 0	in
Pin 21	GND	Signal grounds	
Pin 22	WP	Write Protect	in
Pin 23	GND	Signal grounds	
Pin 24	RDD	Read Data	in
Pin 25	GND	Signal grounds	
Pin 26	HS	Head Select	out

X100 PC/104 BUS interface

Pin	A:	B:	C:	D:
0			Ground	Ground
1	IOCHCK	Ground	SBHE	MEMCS16
2	SD7	RESET	LA23	IOCS16
3	SD6	+5Volt	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	**NC**	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	(-12Volt)	LA18	IRQ14
8	SD1	0WS	LA17	DACK0
9	SD0	+12Volt	MEMR	DRQ0
10	IOCHRDY	Ground **NC**	MEMW	DACK5
11	AEN	SMEMW	SD8	DRQ5
12	SA19	SMEMR	SD9	DACK6
13	SA18	SIOW	SD10	DRQ6
14	SA17	SIOR	SD11	DACK7
15	SA16	DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5Volt
17	SA14	DACK1	SD14	MASTER
18	SA13	DRQ1	SD15	Ground
19	SA12	REF	Ground	Ground
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5Volt		
30	SA1	OSC		
31	SA0	Ground		
32	Ground	Ground		

X101 PC/104+ BUS Interface

Pin	A	B	C	D
1	GND/5.0V KEY2	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	NC
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	NC	PAR
10	GND	NC	+3.3V	NC
11	STOP*	+3.3V	NC	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	NC	Reserved	Reserved	NC

Notes:

1. The shaded area denotes power or ground signals.
2. The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. It is recommended that both KEY pins (A1 and D30) be electrically connected to GND for shielding. **DLAG boards have them as NC (not connected).**

Onboard used signals (not for external use):

IRQ3, IRQ4	COM1 /2
IRQ5	Sound
IRQ7	LPT1
IRQ6	FD
IRQ14	HD
IRQ12	PS/2 Mouse
IRQ13	Coprocessor
TC	FD
DACK2 and DRQ2	FD

X110 LPC-Port

Only for factory and POD-Diagnostic use.

Pin	Signal	Pin	Signal
1	VCC 3.3V	2	LAD0
3	LFrame#	4	LAD1
5	PCI_RST#	6	LAD2
7	FWH_TBL#	8	LAD3
9	VCC 5V	10	PCI_RST#
11	LPC_Clock	12	FWH_Control
13	Ground	14	NC

X230 JTAG-Port

Pin	Signal	Pin	Signal
1	TCK	2	TMS
3	TDI	4	TDO

7. JUMPER LOCATIONS ON THE BOARD

The following figure shows the location of all jumper blocks on the MSB800/L board. The numbers shown in this figure are silk screened on the board so that the pins can easily be located. This chapter refers to the individual pins for these jumpers. The default jumper settings are indicated with asterisks.

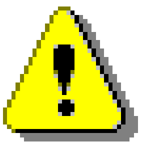
Be careful: some jumpers are soldering bridges; you will need a miniature soldering station with a vacuum pump.

7.1. The Jumpers on MSM800SEV V2.1

Settings written in bold are defaults!

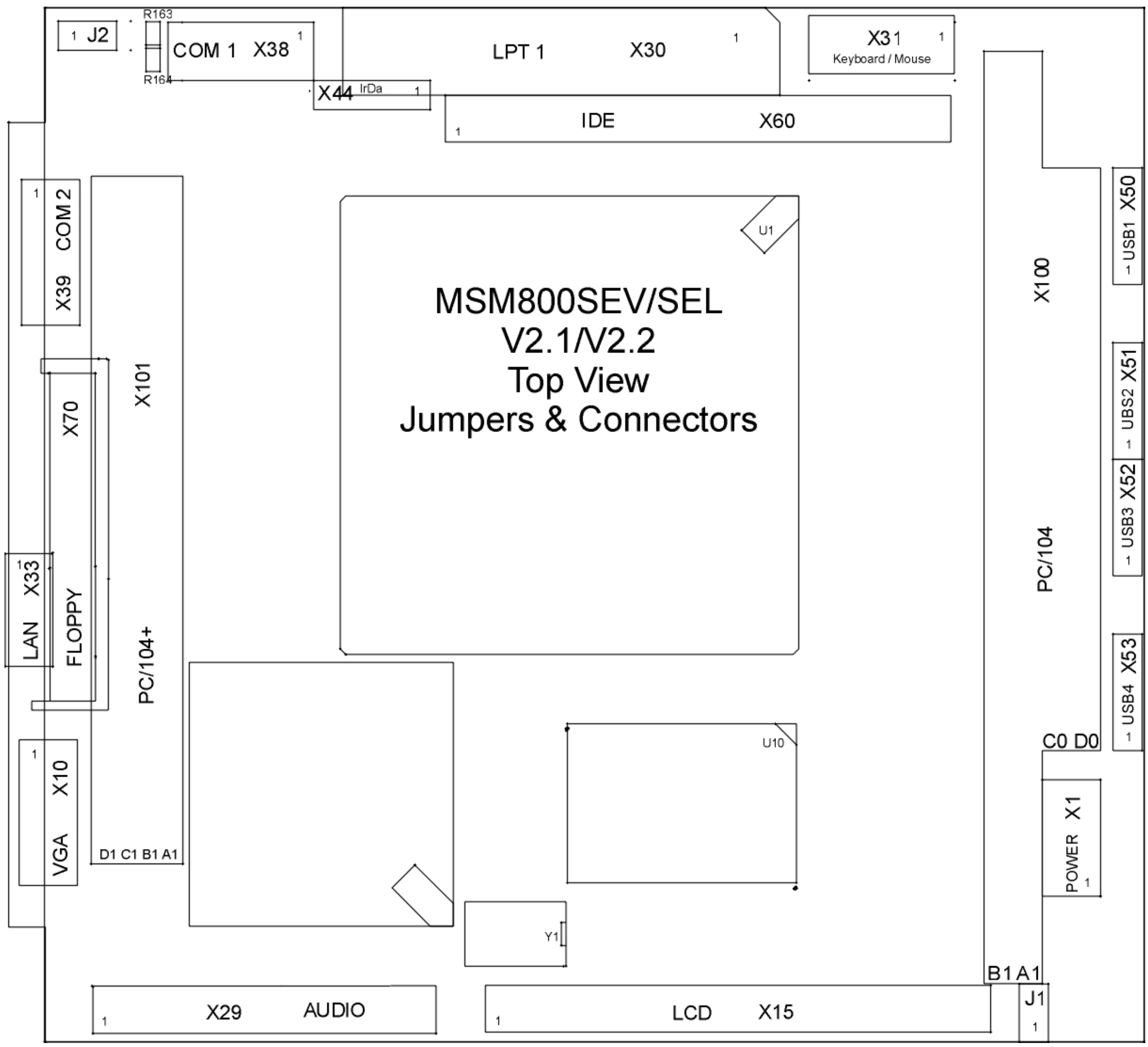
Jumper	Structure	1-2 / open	2-3 / closed	Remarks
J1	Compact Flash select	**Slave**	Master	Top
J2	Power On Switch	Push button	**always** on	Top
J7 [a]	CMOS/EEPROM reset	**Normal function**	Reset	
R163	LCD VDD	5V	**3.3V**	Top
R164	LCD VDD	**3.3V**	5V	Top
R165	LCD BKL (Backlight)	**12V** [b]	5V	Bottom
R166	LCD BKL (Backlight)	5V	**12V** [b]	Bottom

a) For the MSM800BEV/XEV/XEL – refer to Section 4.7.3 for ***important information***!
b) The 12V will not be generated on the board, you must supply the 12V from an external PSU through connector X1 pin4.

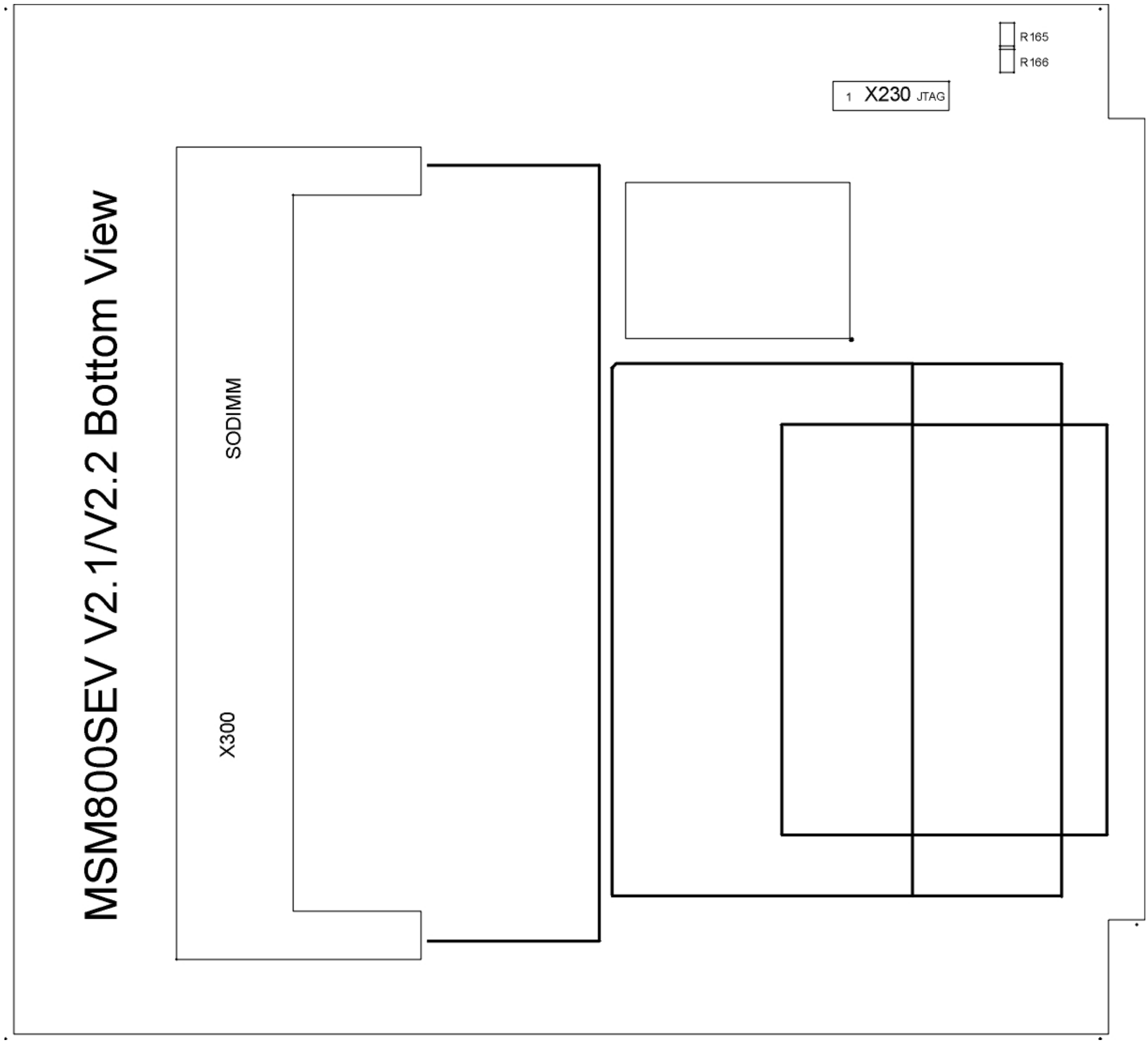


Attention!
Never install R163 and R164 or R165 and R166 together!
The board will be destroyed!

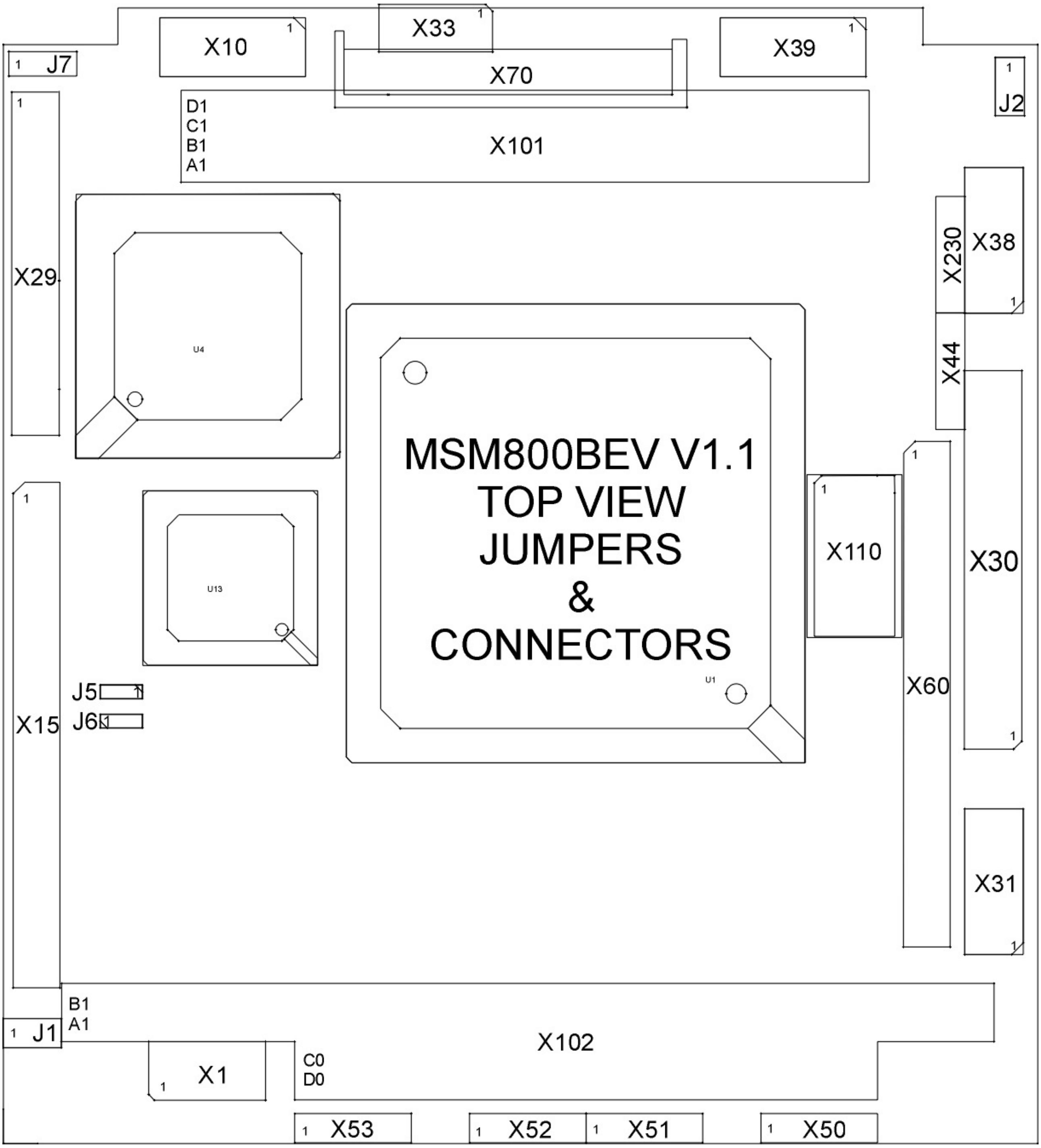
MSM800SEV/SEL V2.1/V2.2 – Top View



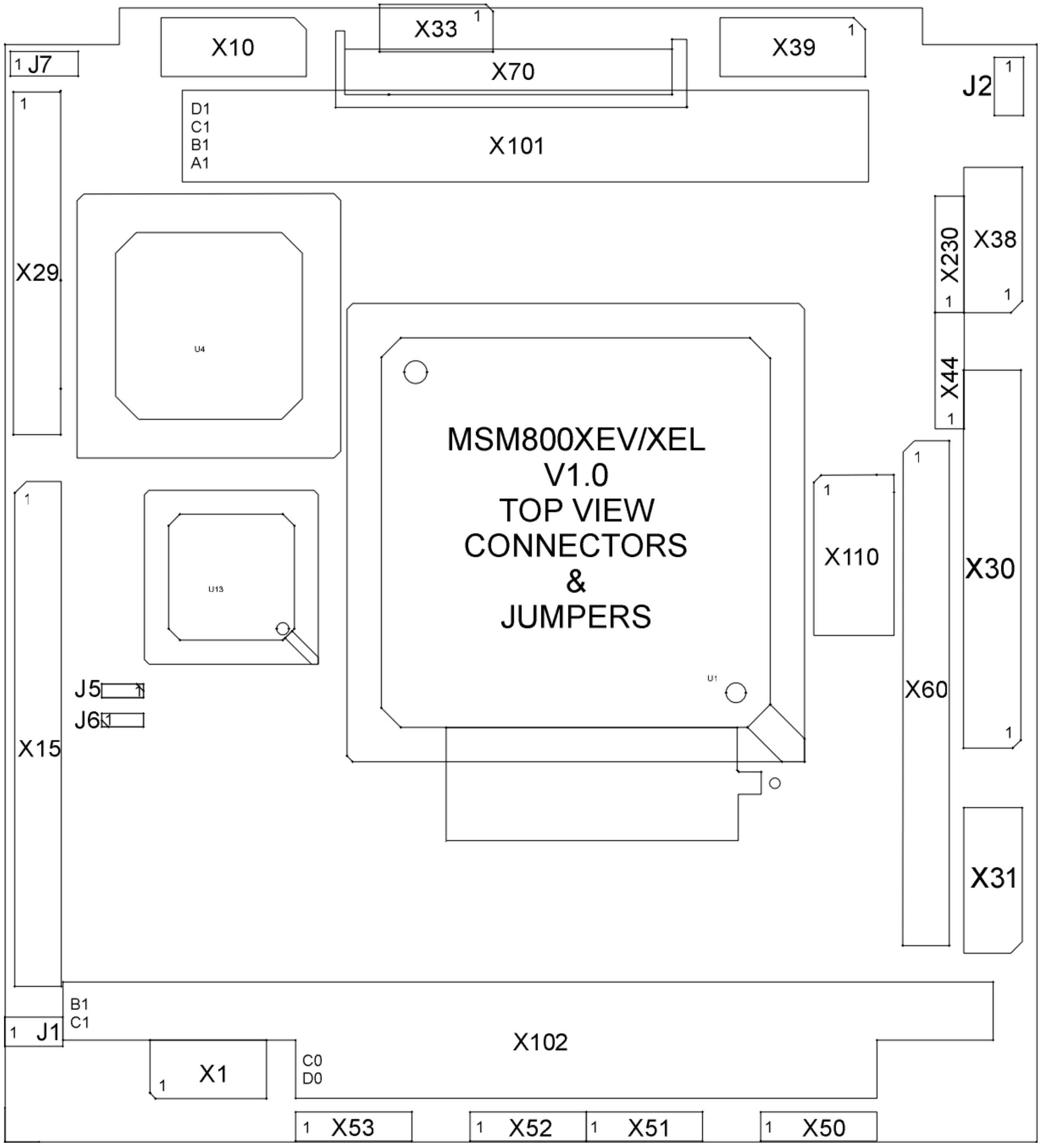
MSM800SEV/SEL V2.1/2.2 – Bottom View



MSM800BEV V1.1 – Top View



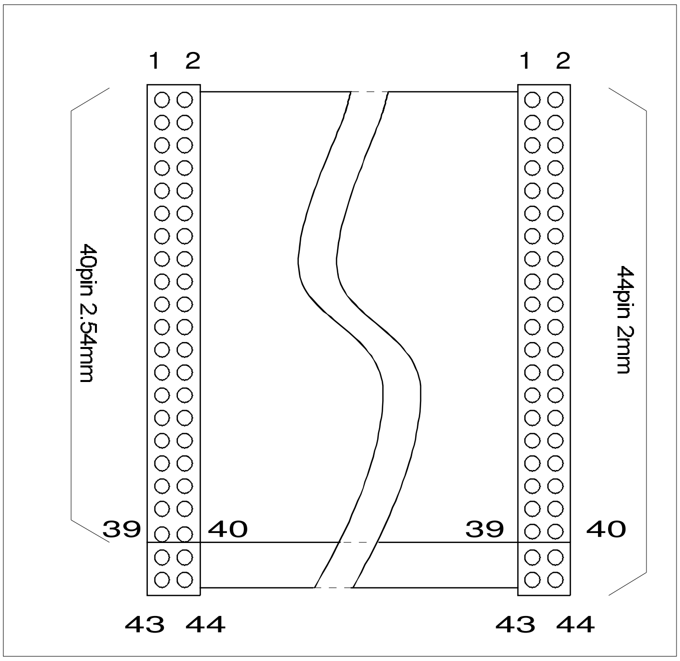
MSM800XEV/XEL V1.0 – Top View



8. CABLE INTERFACES

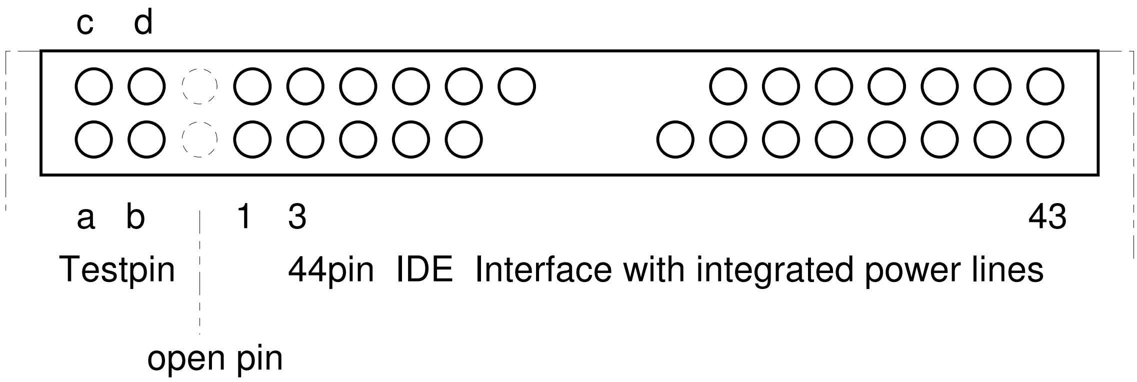
8.1. The Hard Disk Cable 44pin

IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable; 44pins = 40pins signal and 4pins power.



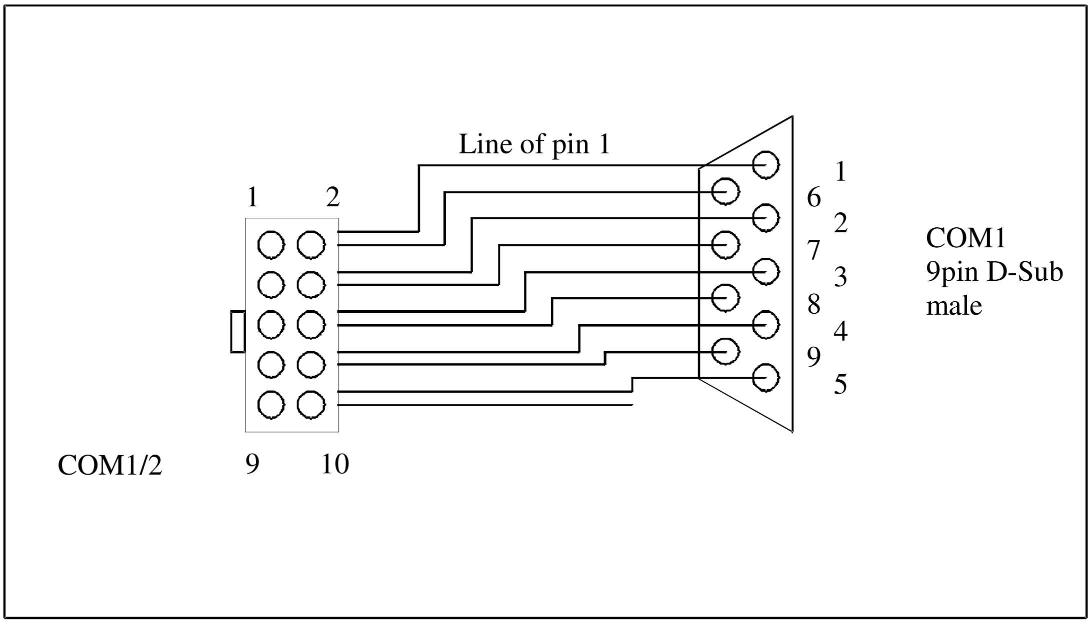
Maximum length for the IDE cable is 30cm.

> ***Attention!***
> Check the pin 1 marker of the cable and the connector before you power-on. Refer to the technical manual of the installed drives because a wrong cable will immediately destroy the drive and/or the MICROSPACE MSM800SEV board. **In this case the warranty is void!** Without the technical manual you may not connect this type of drive.
>
> The 44pin IDE connector on the drives is normally composed of the 44 pins, 2 open pins and 4 test pins, 50 pins in total. Leave the 4 test pins unconnected.



8.2. The COM 1/2 Serial Cable

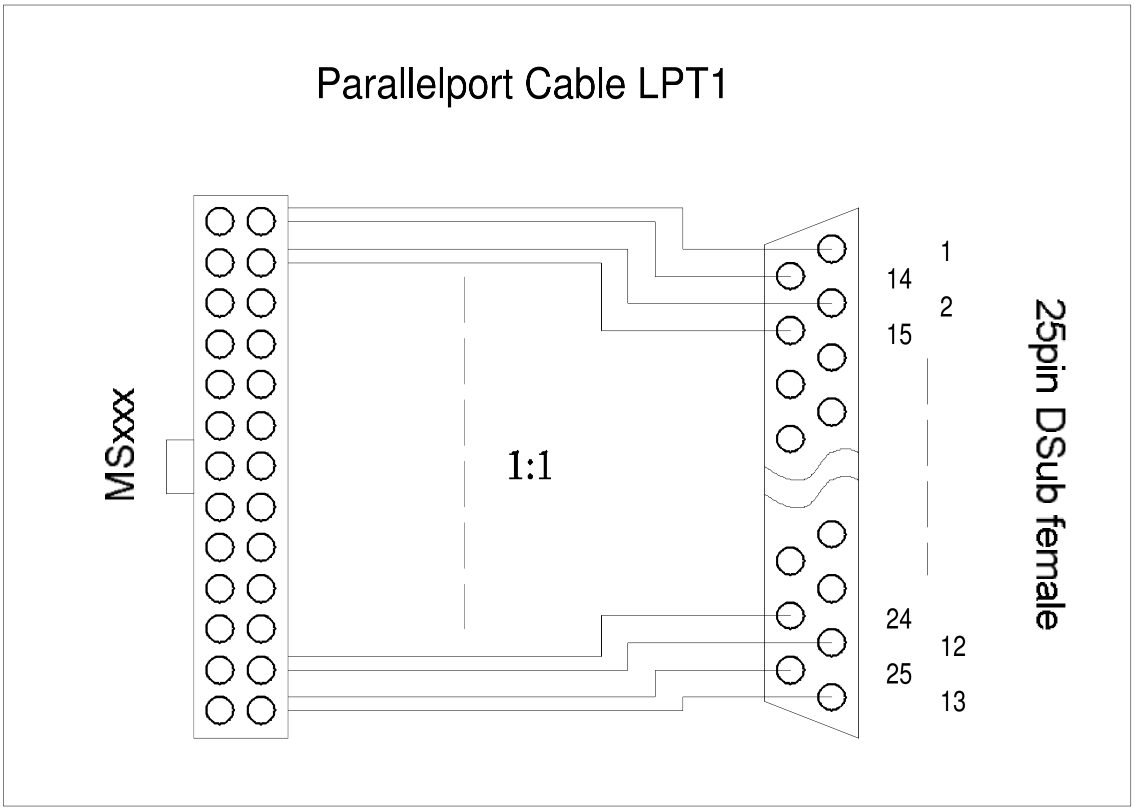
DT terminal for dual row 0.1" (2.54 mm grid) and 1.27 mm flat cable.

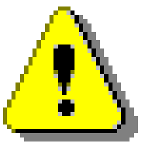


> ***Attention!***
> - Do not short circuit these signal lines.
> - Never connect any pins on the same plug or to any other plug on the MICROSPACE MSM800SEV. The +/- 10Volts will destroy the MICROSPACE core logic immediately**. In this case the warranty is void!**
> - Do not overload the output; the maximum output current converters: 10mA

8.3. The Printer Cable

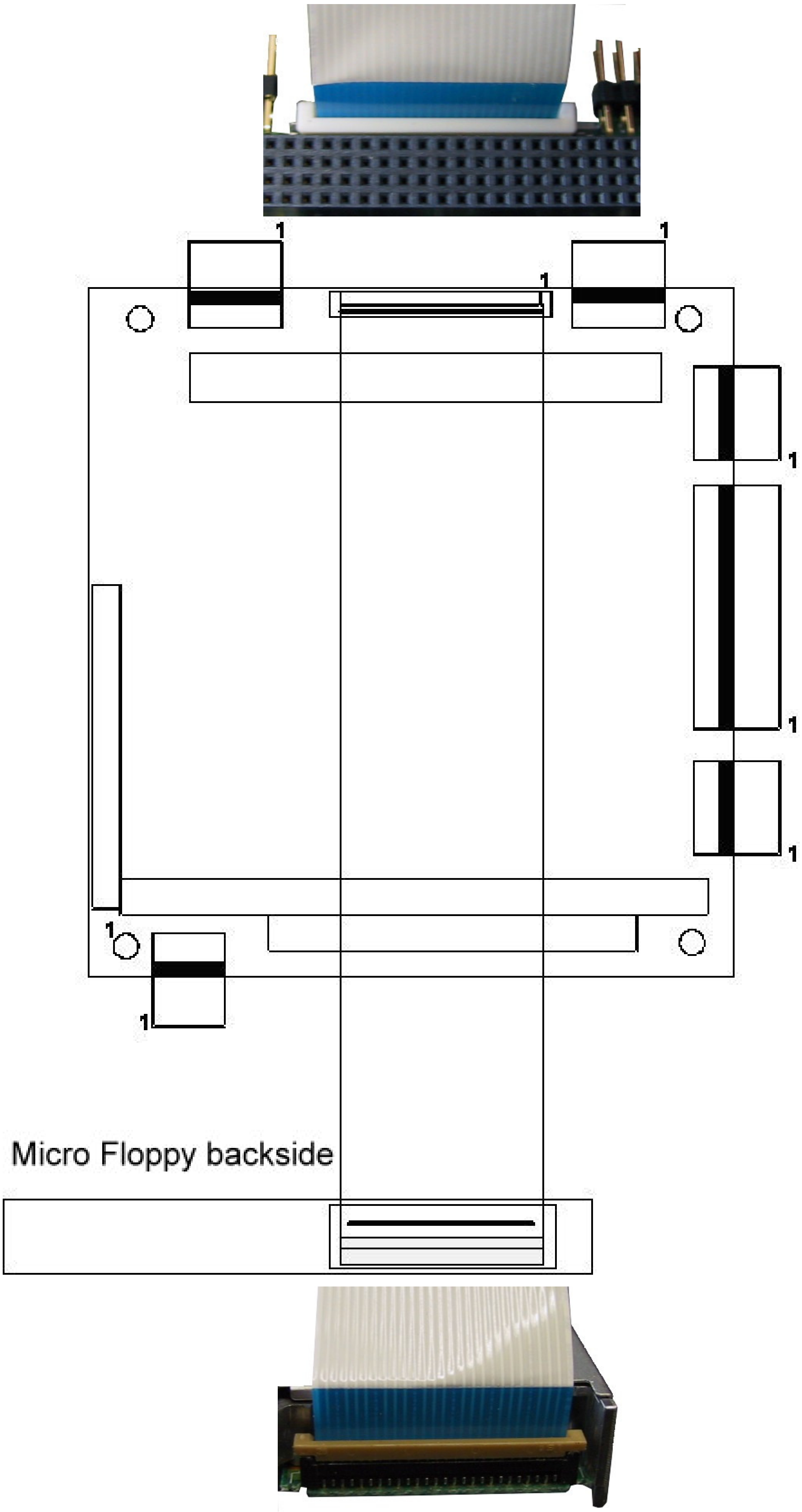
IDT terminal for dual row 0.1" (2.54mm grid) and 1.27 mm flat cable





Attention!
- Maximum length of this cable is 6 meters.
- Prevent short-circuits.
- **Never apply power to these signals, the MICROSPACE MSM800SEV will be destroyed.**

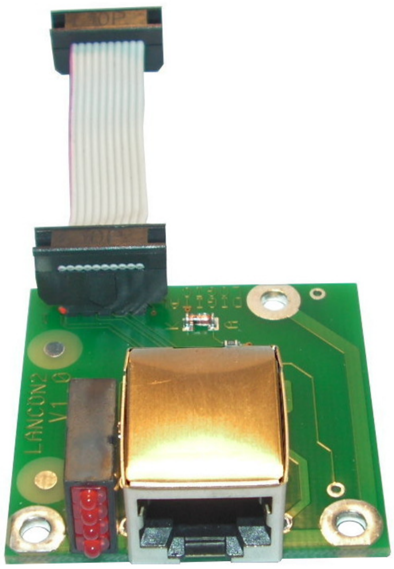
8.4. The Micro Floppy Cable



8.5. The LAN Cable (RJ45)

Attention!
Since board version V2.1 of the MSM800SEV you can not use the MSM855-LANCON anymore, because the LAN transformer (Pulse) is integrated on the PCB.

MSM800SEV V2.1/2.2 = MSM800-LANCON



This picture shows the MSM800-LANCON.

RJ45 connector 10BaseT (IEEE 802.3i), 100BaseTX (IEEE 802.3u):

MDI-Pin	EIA/TIA 568A colors (wire/line)	Pin	Twisted Pair
TX+	White /green	1	3
TX-	Green	2	3
RX+	White/orange	3	2
GND ..		4	1
GND ..		5	1
RX-	Orange	6	2
GND ..		7	4
GND ..		8	4

Cabling:

Do not exceed 100m (328 feet); minimum quality of CAT5, preferably S/FTP or STP CAT6.
Be careful to have a well balanced shield/ground concept.

9. THERMAL SPECIFICATIONS

9.1. Thermal Analysis for Case Integration

Since the integrated heat sink is uni-directional, the airflow must be exactly in the direction of the heat rails. If possible, mount the board vertically, so that the heat rails are up/down. In this case, the self produced airflow is about 3m/sec.

Pay particular attention when mounting the PC-product in a fully enclosed case/box. The thermal energy will be stored in the interior of this environment.

If the case has a fan:

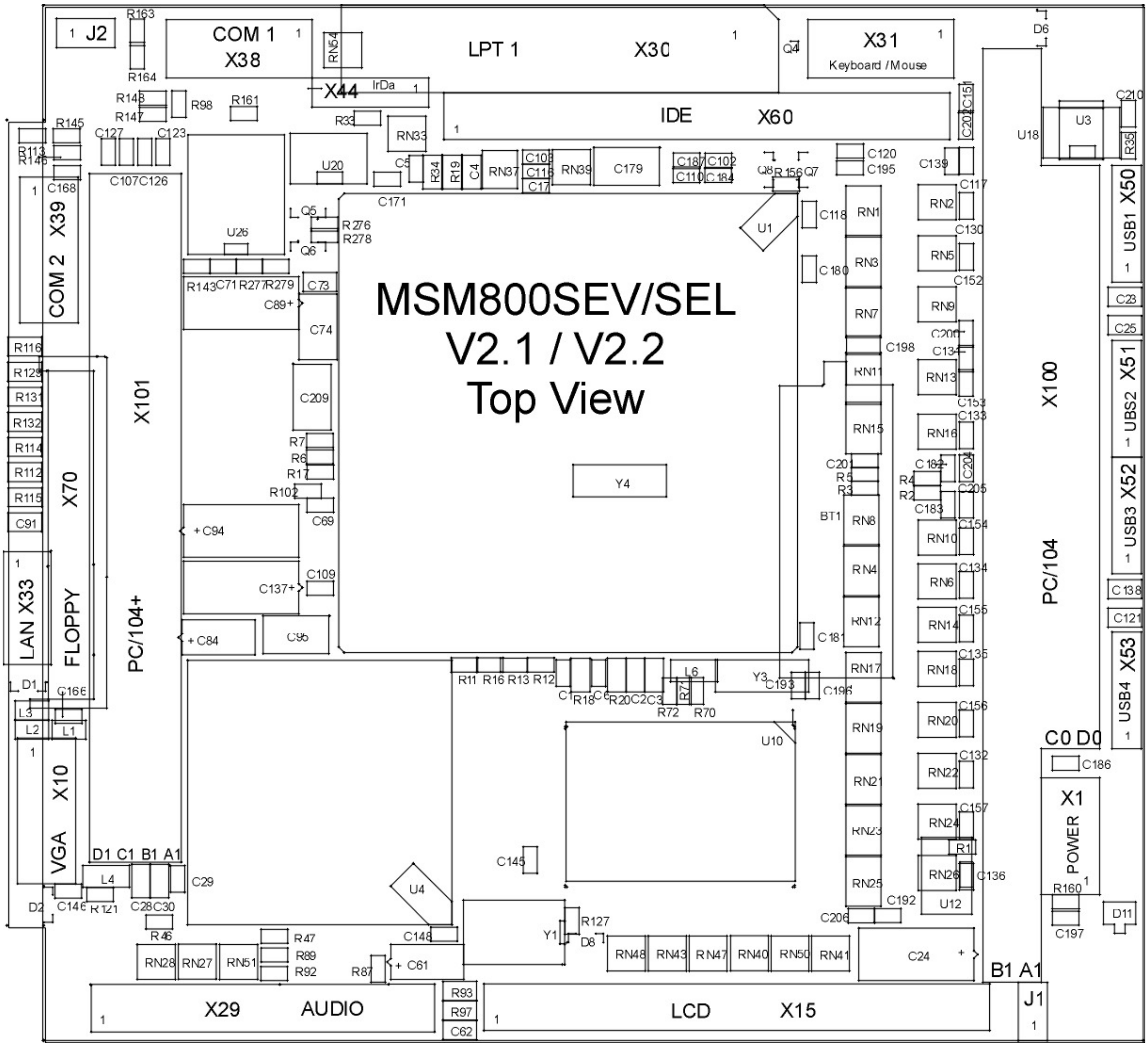
- The hot air must be exchanged with cool air from outside using a filtered fan.
- The hot air must be cooled with a heat exchanger.

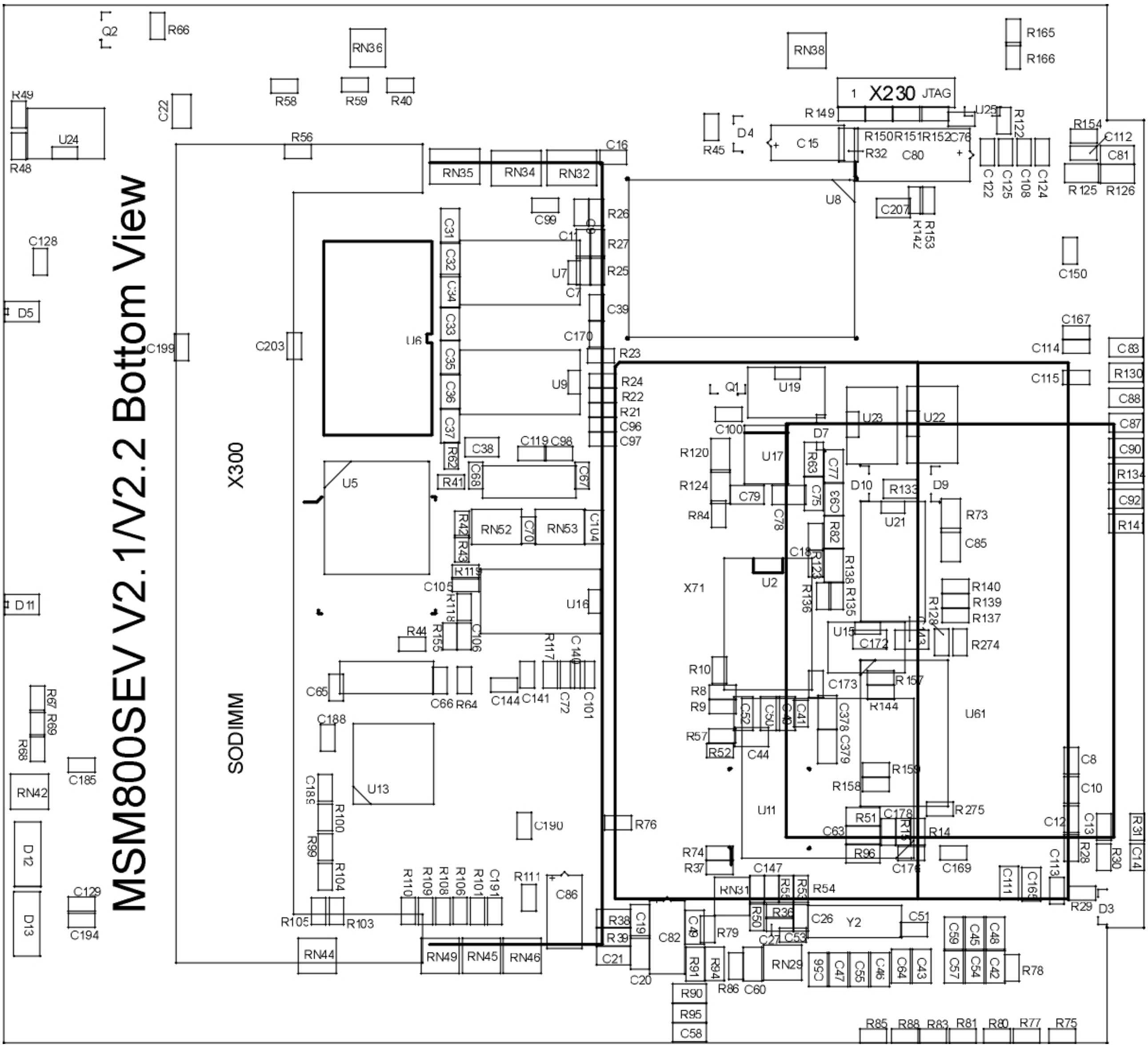
If the case has no fan or opening to exchange the hot air:

- The heat sink of the CPU must be mounted directly to a heat sink integrated into the case. The thermal energy does not go through the air; the heat will be conducted directly through the alloy of the heat sink to the outside.

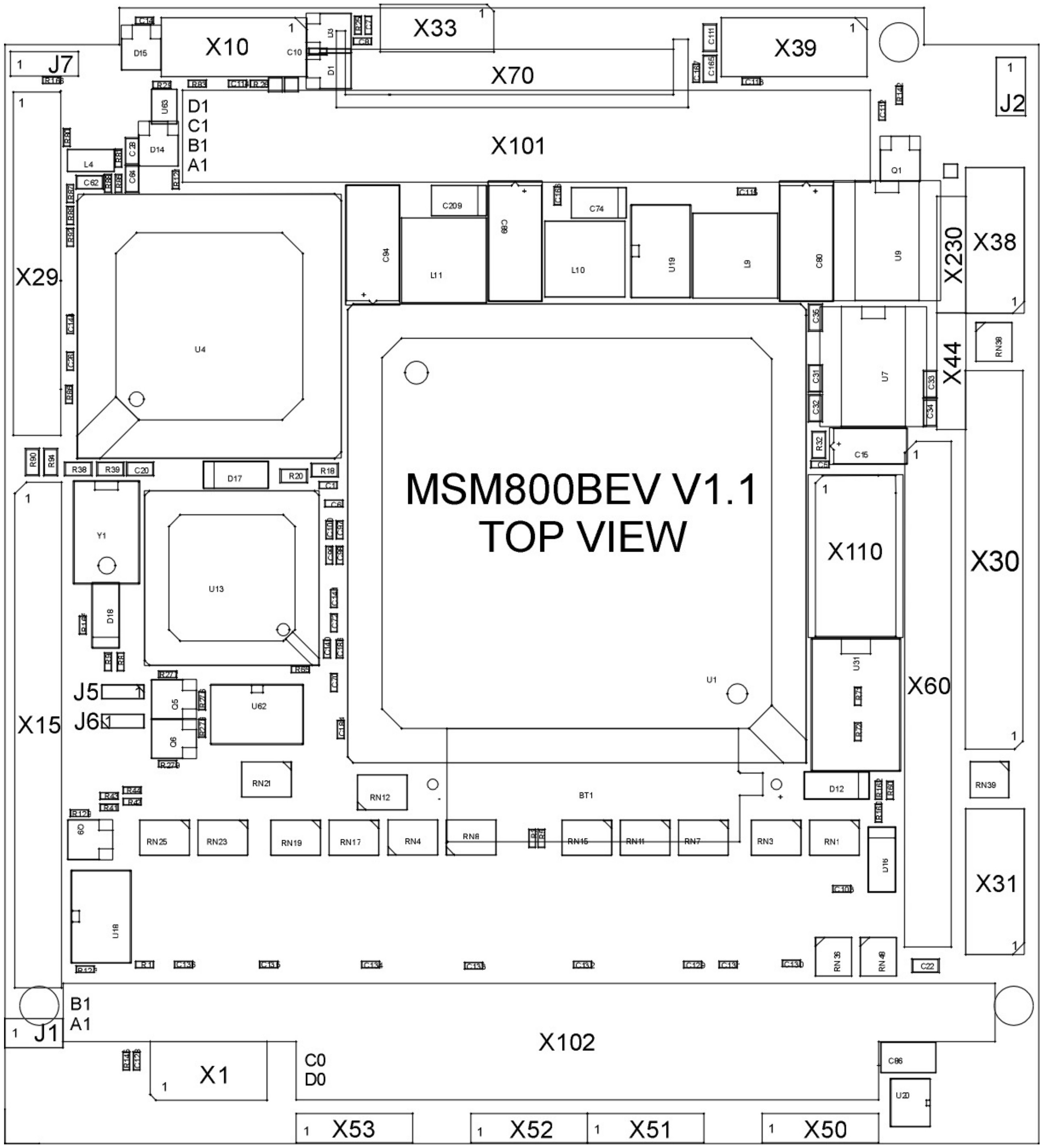
10. ASSEMBLY VIEWS

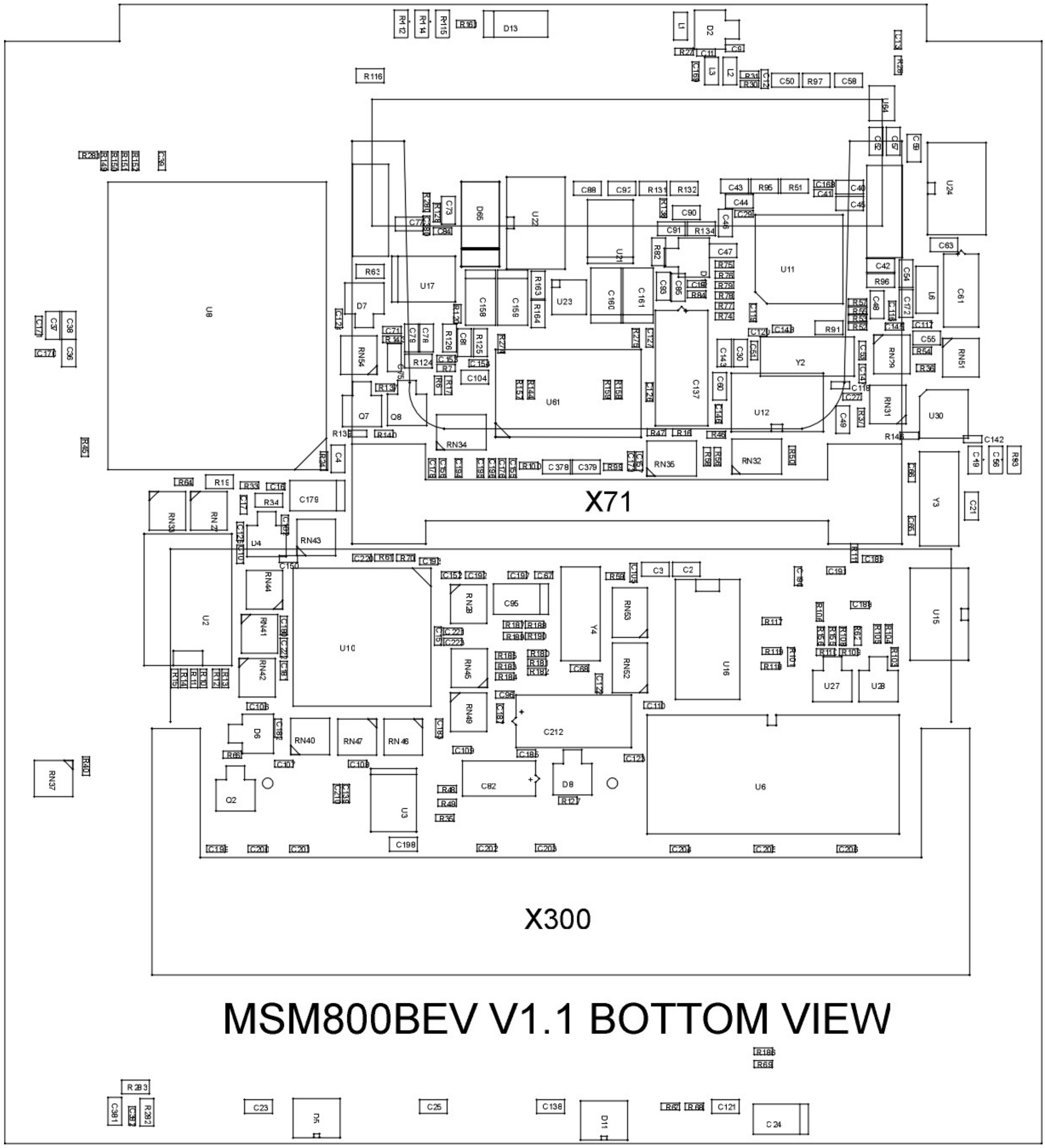
10.1. MSM800SEV/SEL V2.1/V2.2



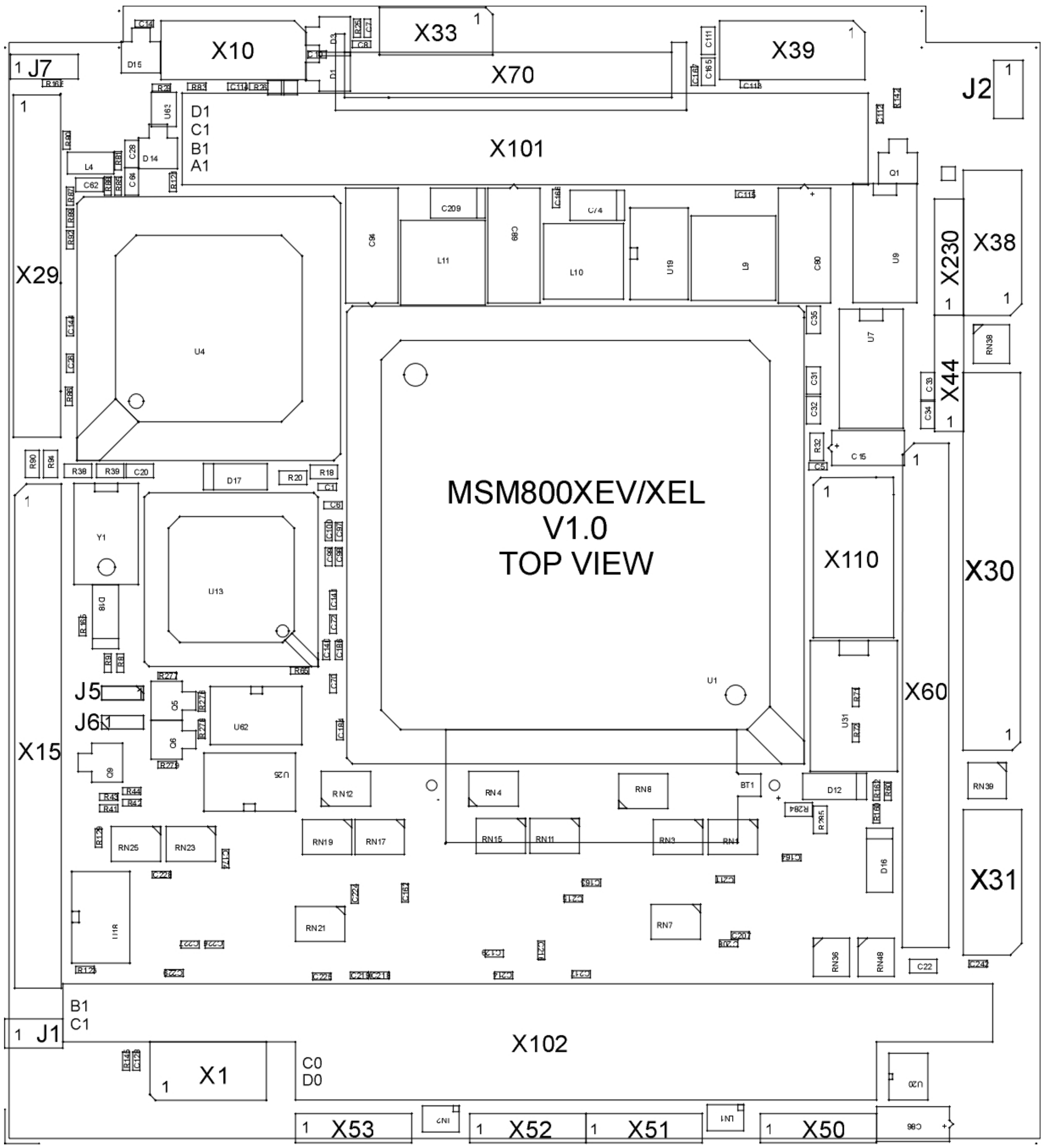

MSM800SEV V2.1/V2.2 Bottom View
X300
SODIMM
X230
JTAG

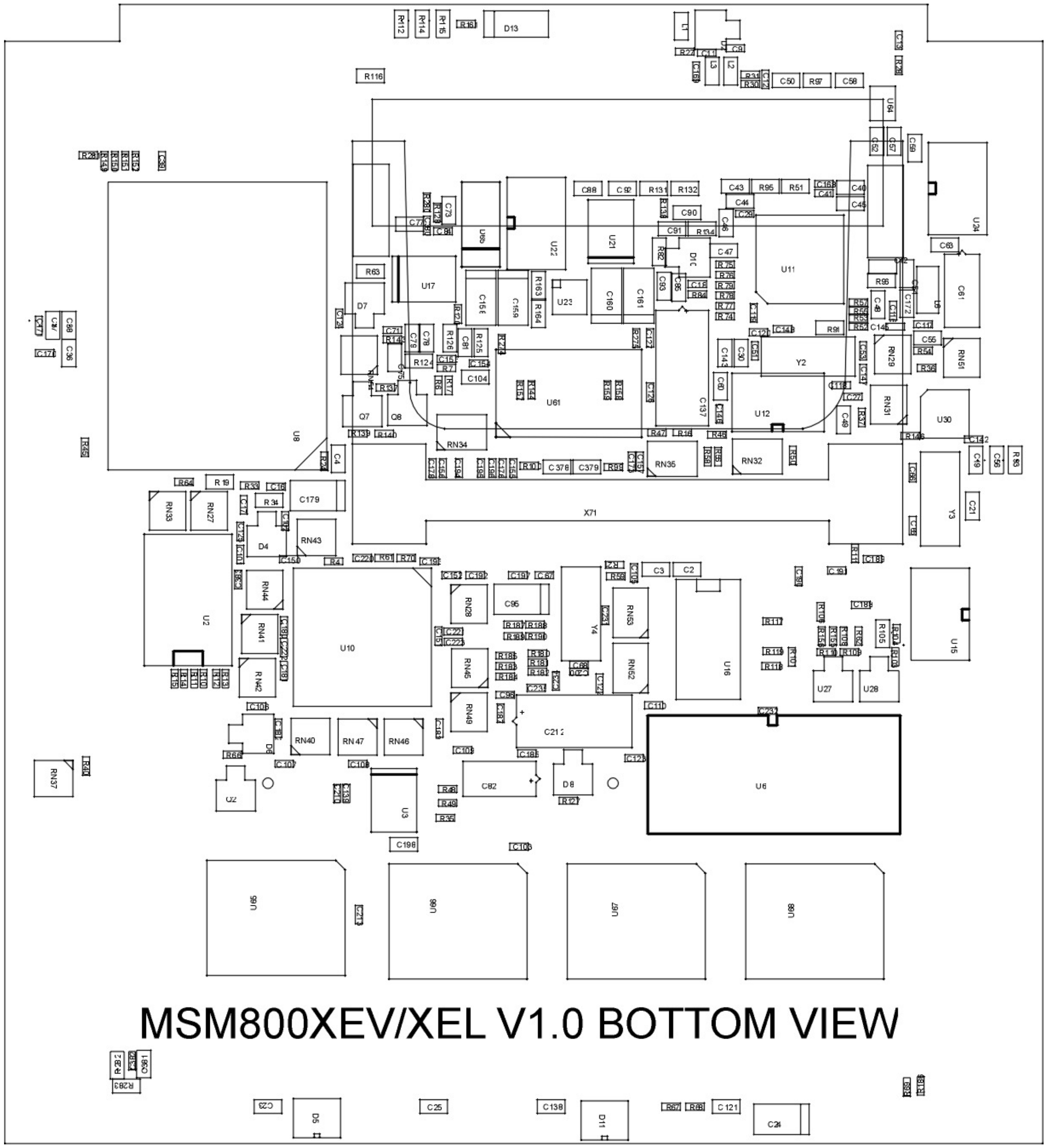
10.2. MSM800BEV V1.1




X71
X300
MSM800BEV V1.1 BOTTOM VIEW

10.3. MSM800XEV/XEL V1.0

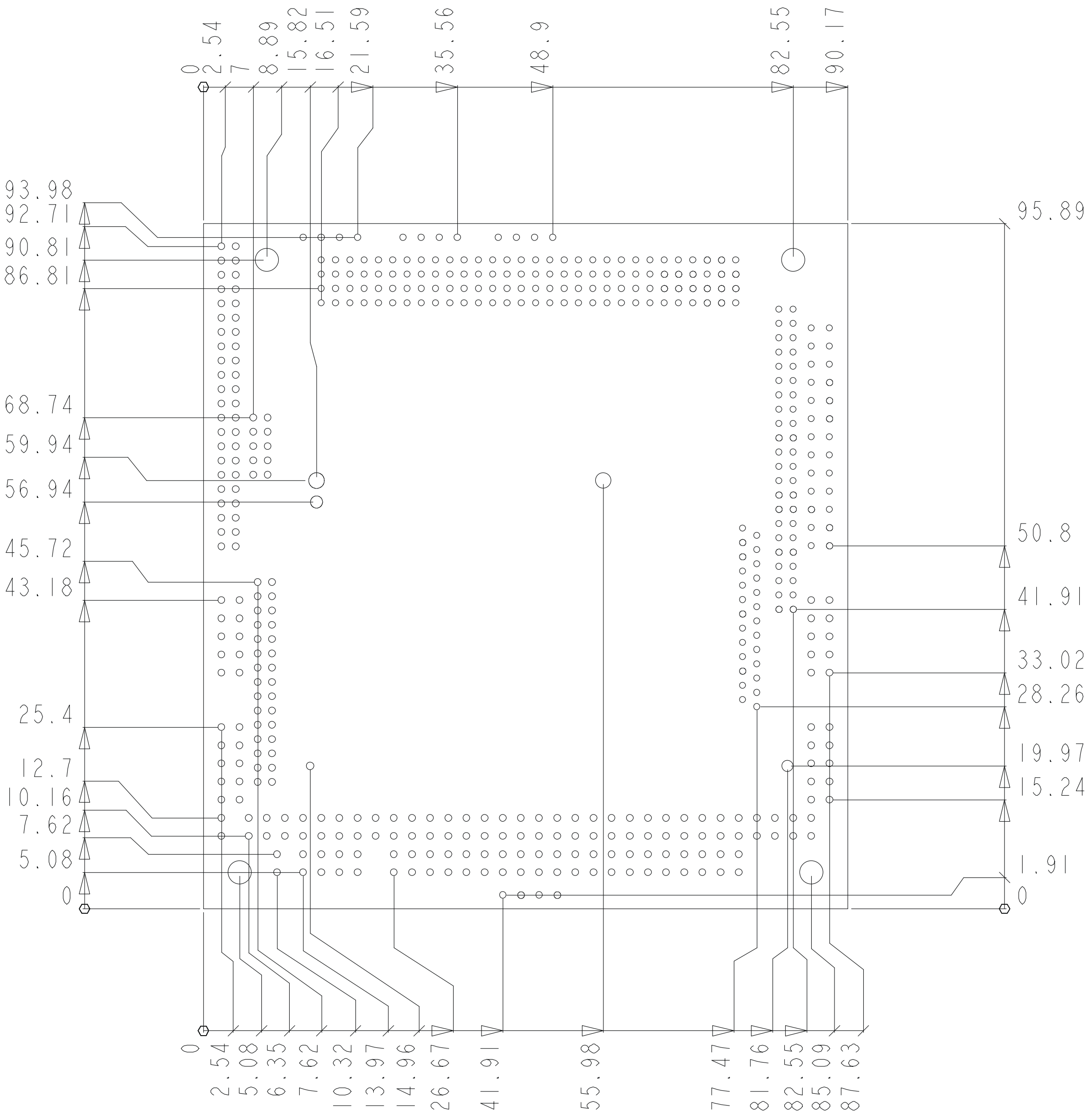




MSM800XEV/XEL V1.0 BOTTOM VIEW

11. PREVIOUS PRODUCT VERSIONS

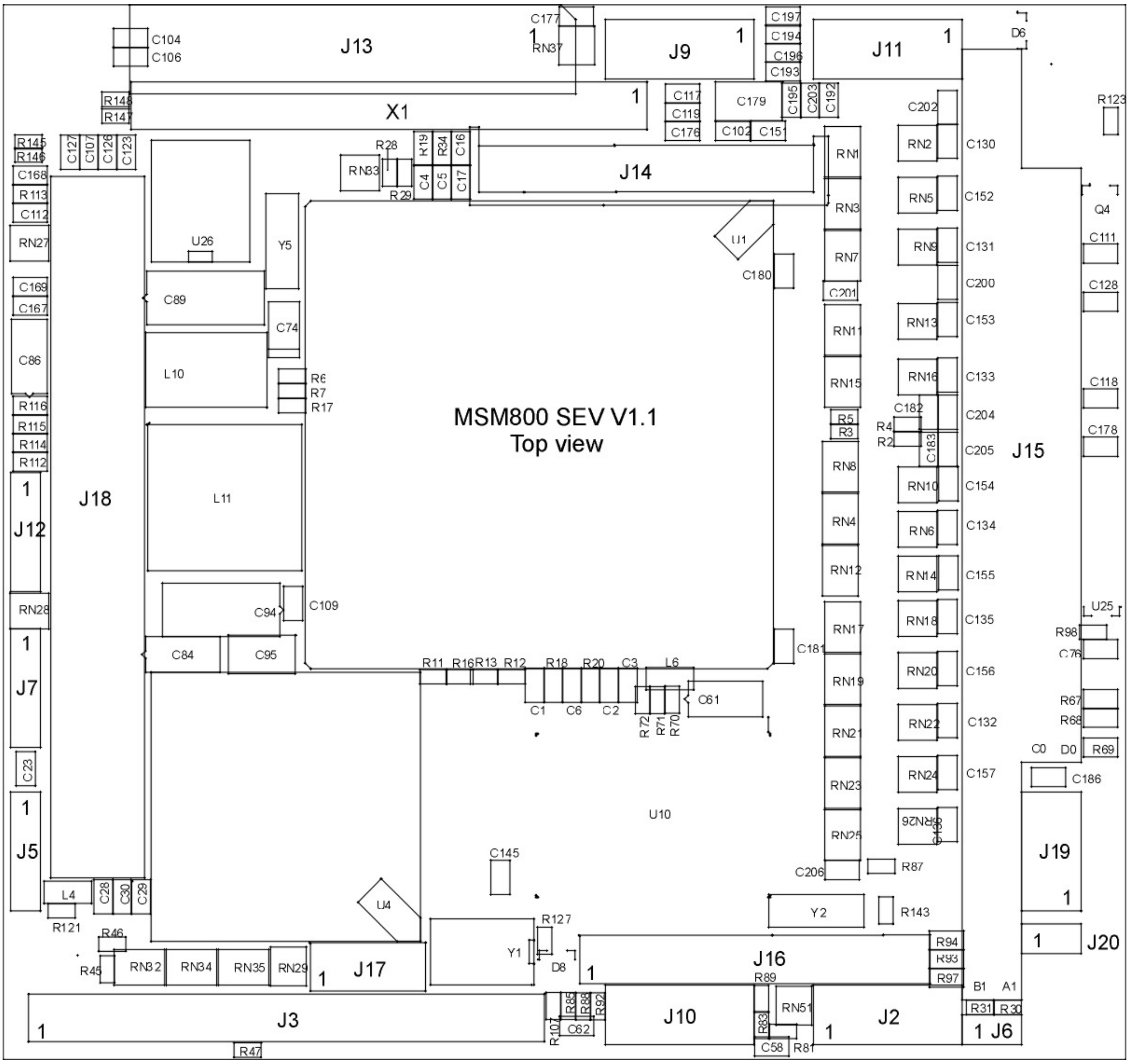
11.1. Board Dimensions – Versions 1.0 / 1.1 / 1.2



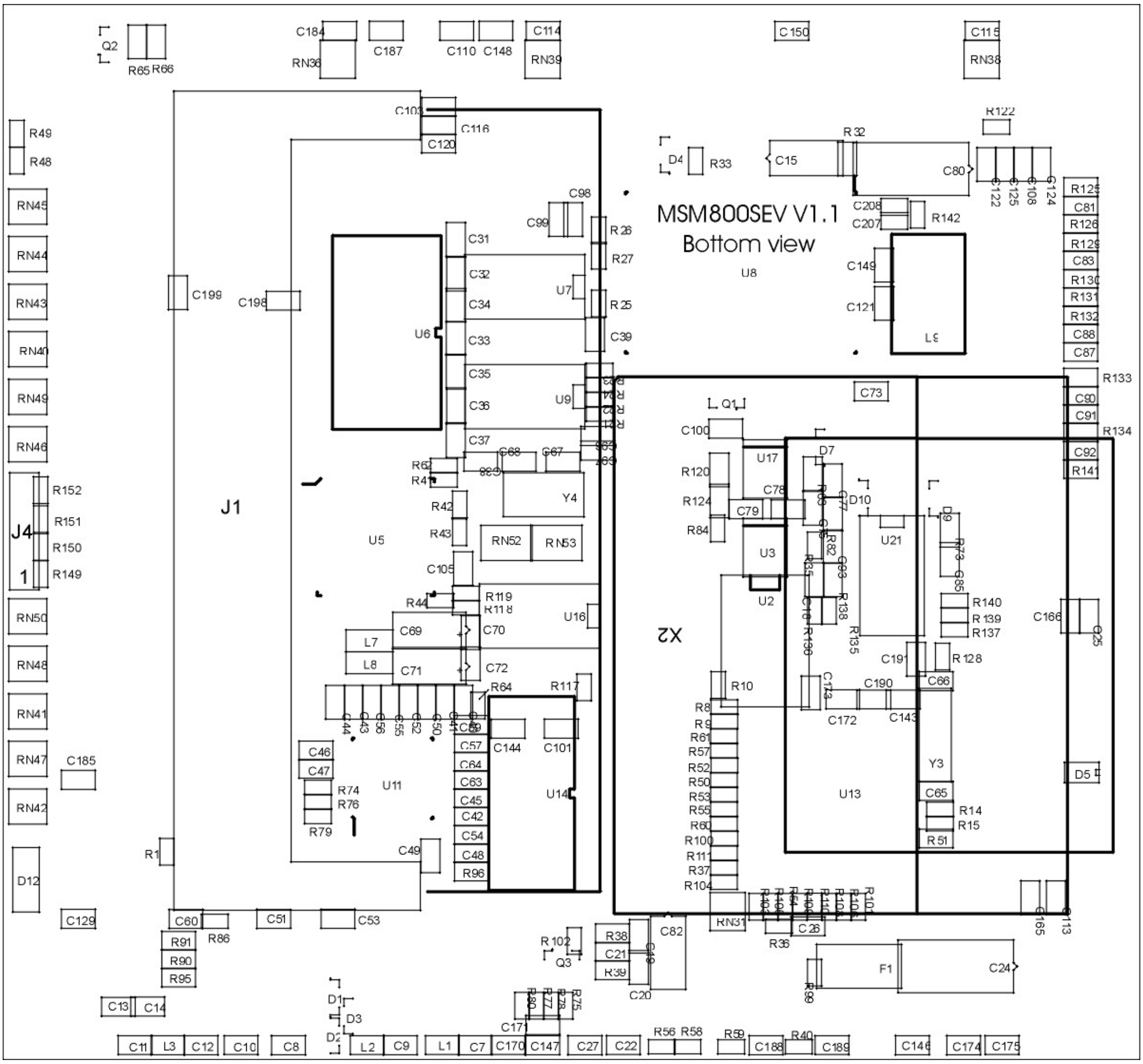
11.2. Assembly Views

11.2.1. MSM800SEV/SEL V1.1

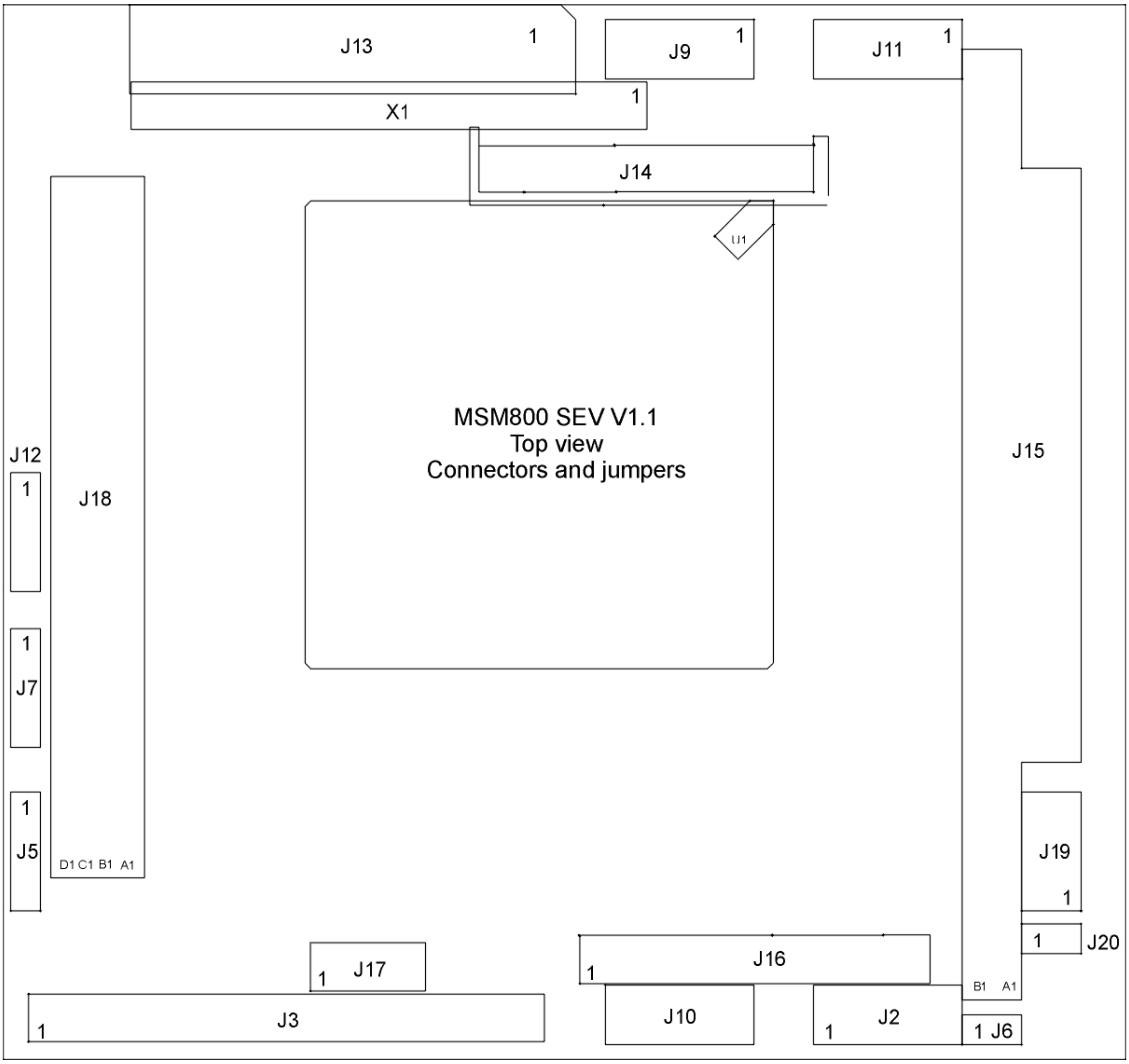
Top View



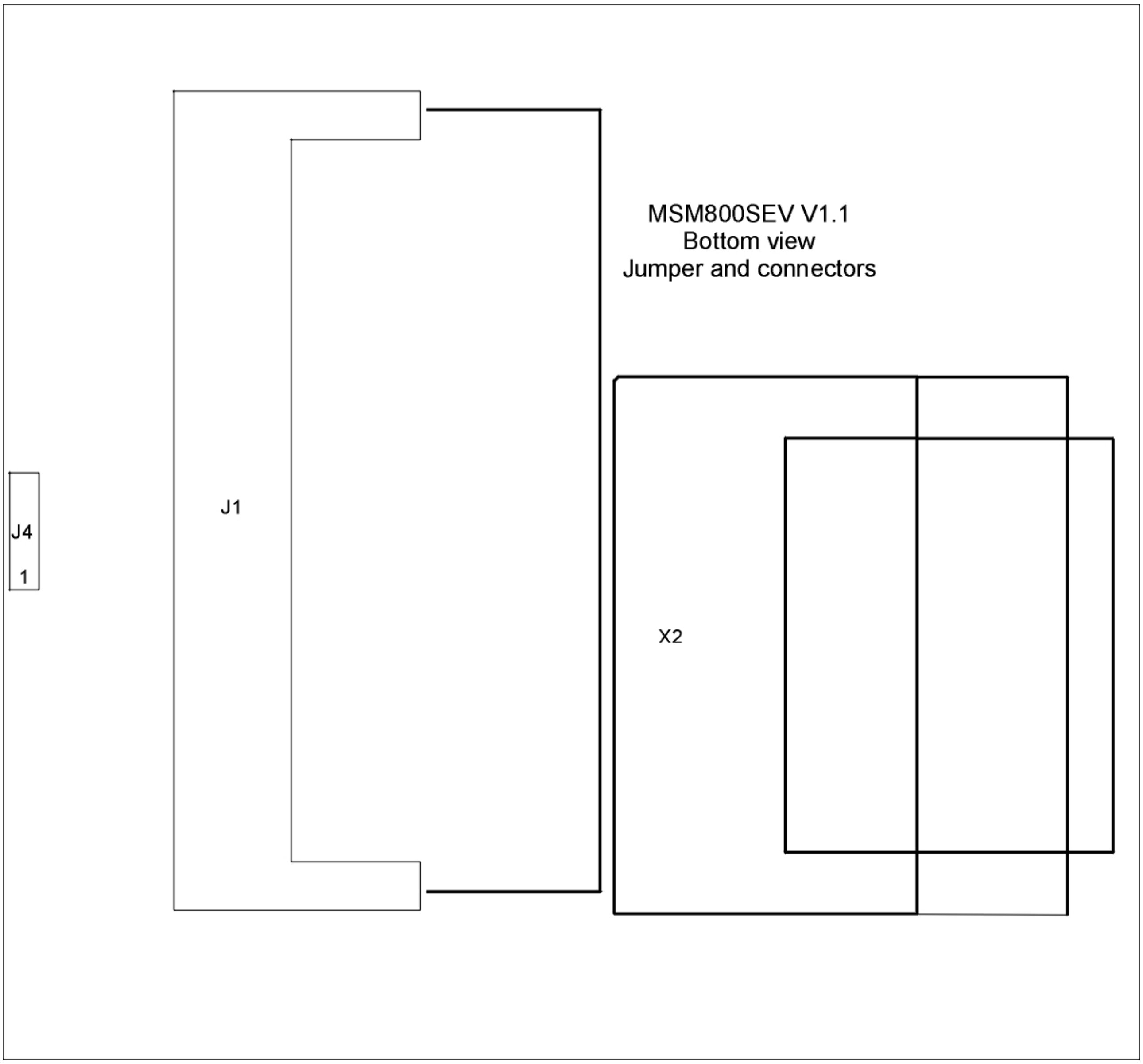
Bottom View



Top View – Connectors and Jumpers

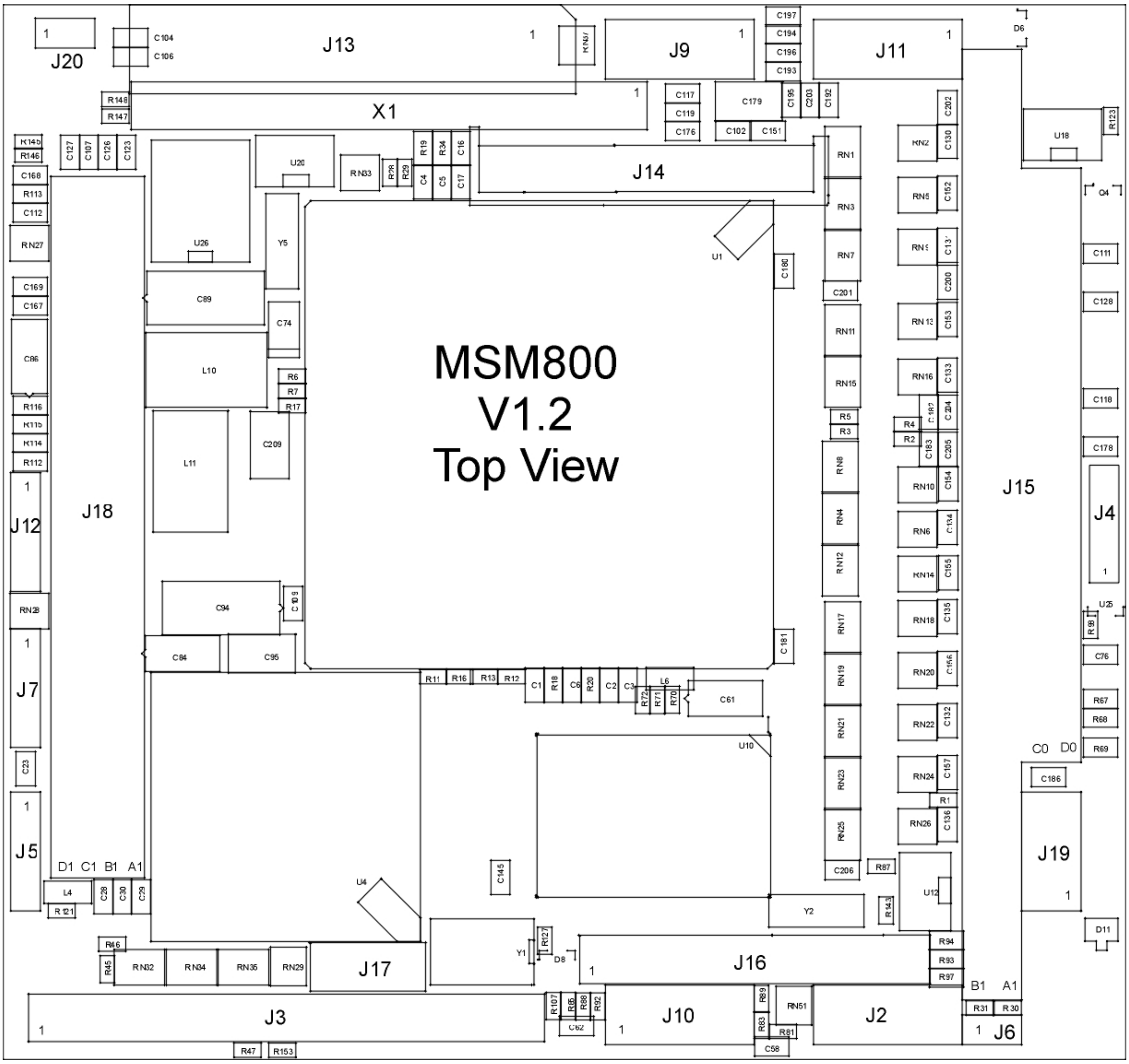


Bottom View – Connectors and Jumpers

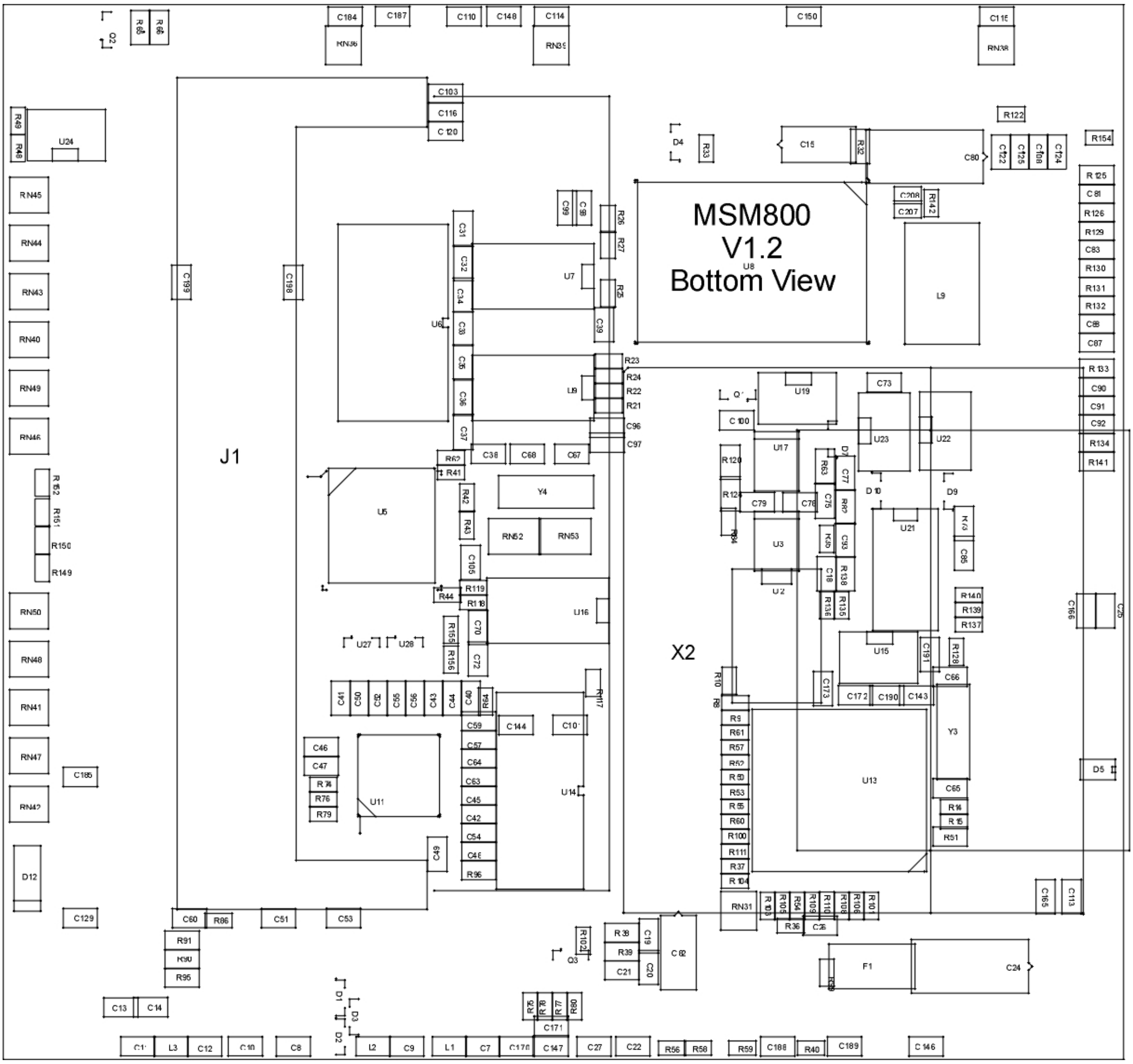


11.2.2. MSM800 V1.2

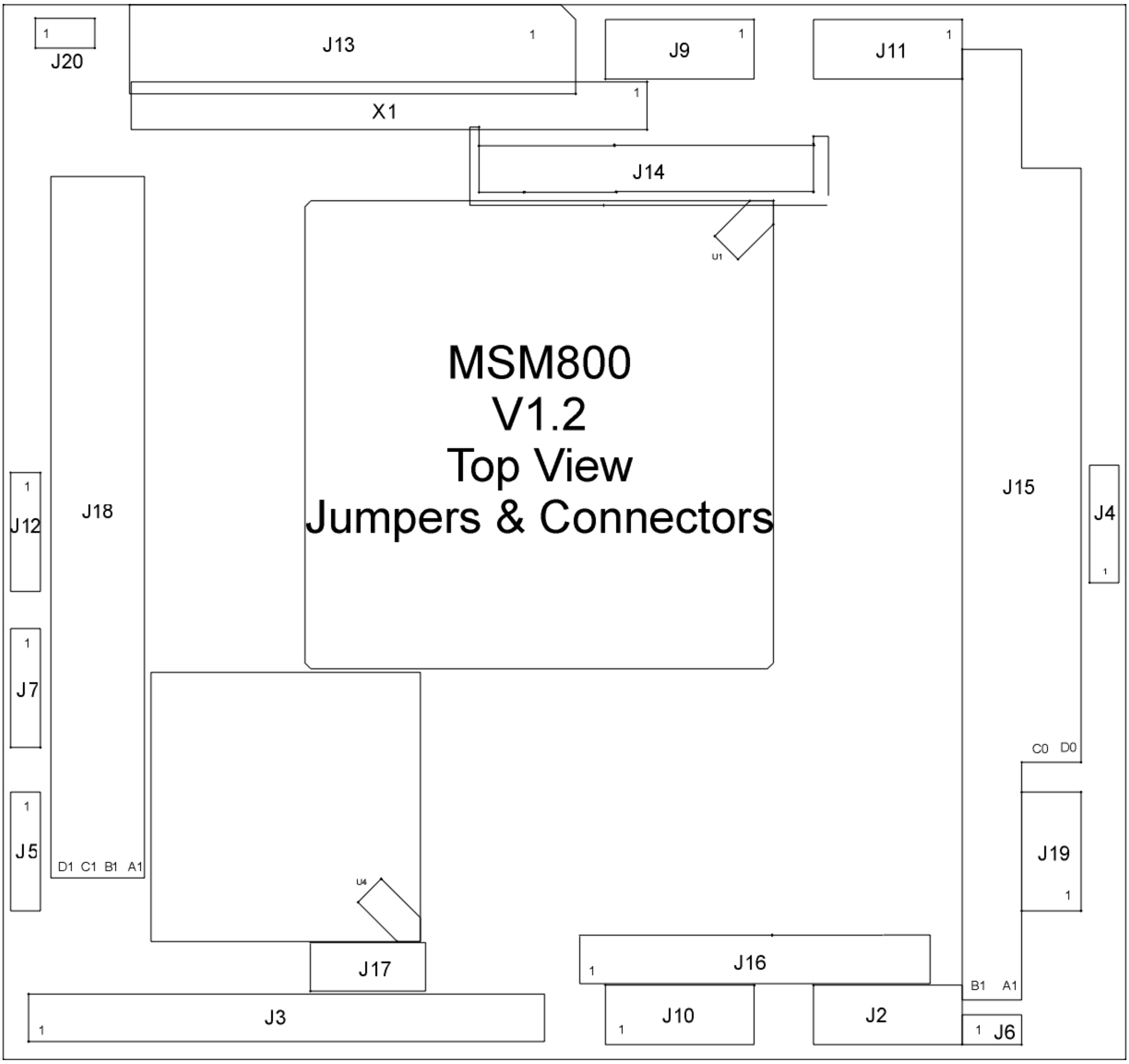
Top View



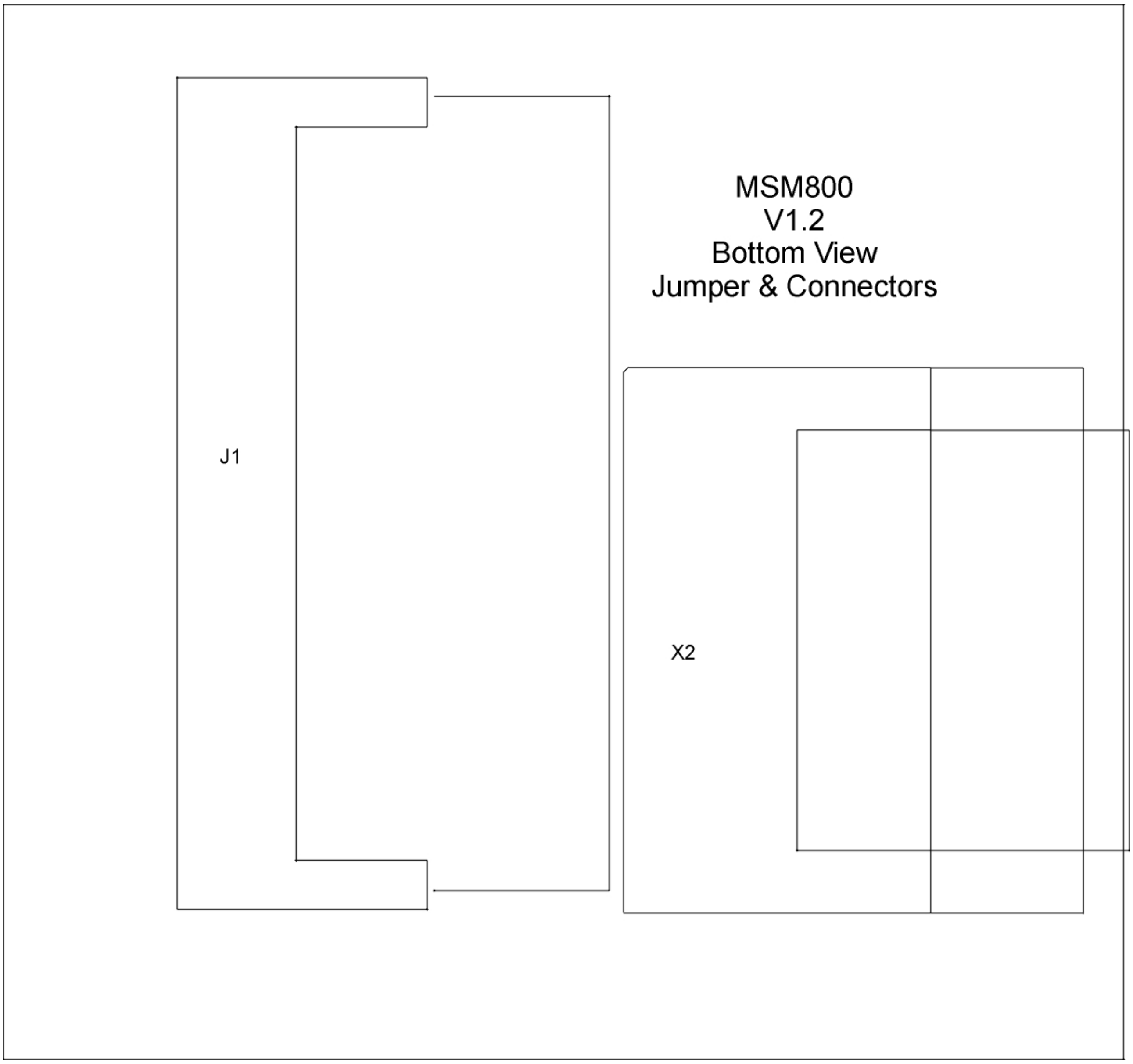
Bottom View



Top View – Connectors and Jumpers



Bottom View – Connectors and Jumpers



11.3. Connectors and Jumpers of Previous Product Versions

11.3.1. Description of the Connectors for V1.0 /V1.1 /V1.2

Flat cable

44pin IDE is:	IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable
All others are:	IDT Terminal for Dual Row 0.1" (2.54mm grid) and 1.27mm flat cable
NC:	not connected

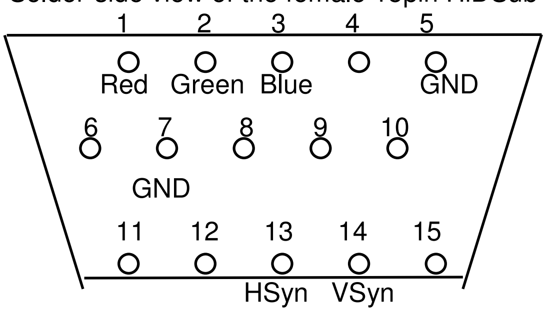
Connector	Structure	Pin	Remarks
J1	PC104+	120	2mm
J2	VGA	2x5	2.54mm
J3	IDE	2x22	2mm
J4	JTAG-Port	4	2.54mm
J5	USB 1	4	2.54mm
J7	USB 2	4	2.54mm
J9	COM1	2x5	2.54mm
J10	COM2	2x5	2.54mm
J11	Keyboard, mouse, utility	2x5	2.54mm
J12	IrDA	4	2.54mm
J13	LPT1	2x13	2.54mm
J14	Floppy	26	FCC micro
J15	PC104	104	2.54mm
J16	Sound Audio I/O	2x15	2.00mm
J17	LAN / Battery	2x5	2.00mm
J19	Power, PM	2x4	2.54mm
U1	SODIMM	144	0.8mm
X1	LCD	2x22	2mm
X2	Compact Flash Holder		

J2 VGA Monitor (CRT-signals)

J2 Header		15 pins HiDensity DSUB	
10 Pin -M	Signal	Pin	Signal
2	VGA red	1	Red
4	VGA green	2	Green
6	VGA blue	3	Blue
8	Horizontal Synch	13	H-Synch
9	Vertical Synch	14	V-Synch
		5 + 11	Bridged
1	Ground	5, 6, 7, 8	Ground
3	NC		
5	NC		
7	Serial_Data		
10	Serial_Clock		

The VGA-CRT signals from J2 must be wired to a standard VGA HiDensity DSub connector (female):
The LCD signals must be wired panel specific.

Solder-side view of the female 15pin HiDSub



J3. IDE Interface

Pin	Signal	Pin	Signal
1	= Reset (active low)	2	= GND
3	= D7	4	= D8
5	= D6	6	= D9
7	= D5	8	= D10
9	= D4	10	= D11
11	= D3	12	= D12
13	= D2	14	= D13
15	= D1	16	= D14
17	= D0	18	= D15
19	= GND	20	= (keypin) NC
21	= DREQ	22	= GND
23	= IOW (active low)	24	= GND
25	= IOR (active low)	26	= GND
27	= IORDY	28	= ALE / Master-Slave
29	= DACK	30	= GND
31	= IRQ14	32	= NC
33	= ADR1	34	= NC
35	= ADR0	36	= ADR2
37	= CS0 (active low)	38	= CS1 (active low)
39	= LED (active low)	40	= GND
41	= VCC Logic	42	= VCC Motor
43	= GND	44	= NC

J4 JTAG-Port

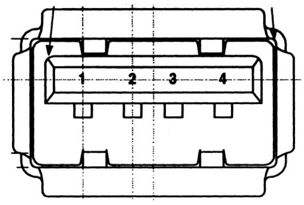
Pin	Signal	Pin	Signal
1	TCK	2	TMS
3	TDI	4	TDO

J5 USB 1 Connector

Pin	Signal
1	= VCC
2	= USB-P0-
3	= USB-P0+
4	= GND

J7 USB 2 Connector

Pin	Signal
1	= VCC
2	= USB-P0-
3	= USB-P0+
4	= GND



Pin 1	= VCC
Pin 2	= USB-P0-
Pin 3	= USB-P0+
Pin 4	= GND

J8 LPC-Port

Only for factory and POD-Diagnostic use.

Pin	Signal	Pin	Signal
1	VCC 3.3V	2	LAD0
3	LFrame#	4	LAD1
5	PCI_RST#	6	LAD2
7	FWH_TBL#	8	LAD3
9	VCC 5V	10	PCI_RST#
11	LPC_Clock	12	NC
13	Ground	14	FWH_Control

J9 Serial Port COM1

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= DCD
Pin 2	Pin 6	= DSR
Pin 3	Pin 2	= RxD
Pin 4	Pin 7	= RTS
Pin 5	Pin 3	= TxD
Pin 6	Pin 8	= CTS
Pin 7	Pin 4	= DTR
Pin 8	Pin 9	= RI
Pin 9	Pin 5	= GND
Pin 10		= open

J10 Serial Port COM2

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= DCD
Pin 2	Pin 6	= DSR
Pin 3	Pin 2	= RxD
Pin 4	Pin 7	= RTS
Pin 5	Pin 3	= TxD
Pin 6	Pin 8	= CTS
Pin 7	Pin 4	= DTR
Pin 8	Pin 9	= RI
Pin 9	Pin 5	= GND
Pin10		= open

J11 Keyboard PS/2/-Mouse Utility Connector

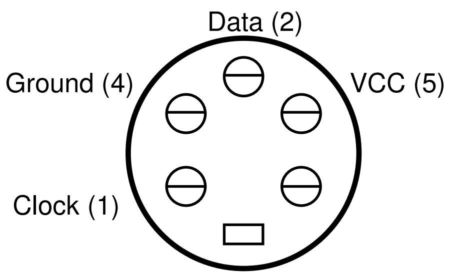
The speaker must be connected to VCC, to have a low inactive current in the speaker !

Pin	Signal	Pin	Signal
1	= Speaker Out	2	= Ground (for Speaker)
3	= Reset In (activ low)	4	= VCC
5	= Keyboard Data	6	= Keyboard Clock
7	= Ground	8	= Ext. Lithium battery
9	= PS/2 Mouse Clock	10	= PS/2 Mouse Data

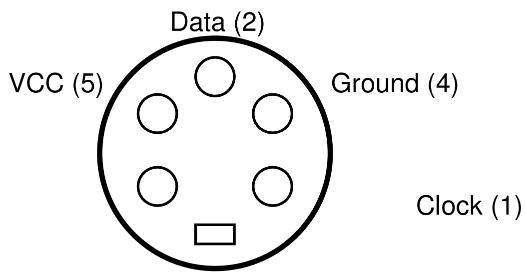
Reset-In-Signal has an internal Pullup of 1k to 5Volt VCC.

The Utility connector must be wired to a standard AT-female connector:

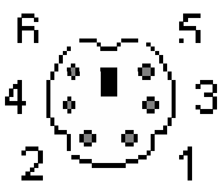
Front side AT-Keyboard (female)



Solder-side AT-Keyboard (female)



PS/2 Front side (female)



Connector and adapter

	Mini-DIN PS/2 (6 PC)	DIN 41524 (5 PC)	Remarks
Shield	Shield	Shield	KEYBOARD
DATA	1	2	
GND	3	4	
VCC (+5V)	4	5	
CLK	5	1	
	Mini-DIN PS/2 (6 PC)		
VCC (+5V)	4		MOUSE
DATA	1		
GND	3		
CLK	5		

J12 IrDA Connector

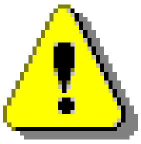
Pin	Signal
1	VCC
2	IRTX
3	IRRX
4	GND

BIOS settings:

You must enable the UART A of the GeodeLX in the BIOS setup:

F1→Mother board device configuration→I/O configuration:

- UART port A = enabled
- UART mode = SIR/CIR



Attention!

Never set the UART A mode to “Serial-16550 compatible” or “Extended” when an IrDA diode is connected to the X44 or **the diode will be destroyed!**

J13. Printer Port (Centronics)

The printer connector provides an interface for 8bit Centronics printers.

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= Strobe
Pin 3	Pin 2	= Data 0
Pin 5	Pin 3	= Data 1
Pin 7	Pin 4	= Data 2
Pin 9	Pin 5	= Data 3
Pin 11	Pin 6	= Data 4
Pin 13	Pin 7	= Data 5
Pin 15	Pin 8	= Data 6
Pin 17	Pin 9	= Data 7
Pin 19	Pin 10	= Acknowledge
Pin 21	Pin 11	= Busy
Pin 23	Pin 12	= paper end
Pin 25	Pin 13	= select
Pin 2	Pin 14	= autofeed
Pin 4	Pin 15	= error
Pin 6	Pin 16	= init printer
Pin 8	Pin 17	= shift in (SI)
Pins 10, 12, 14, 16, 18	Pins 18-22	= left open
Pins 20, 22, 24	Pins 23-25	= GND

J14. Floppy Disk interface connector

FD26	Signal Name	Function	in/out
Pin 1	VCC	+5 volts	
Pin 2	IDX	Index Pulse	in
Pin 3	VCC	+5 volts	
Pin 4	DS2	Drive Select 2	out
Pin 5	VCC	+5 volts	
Pin 6	DCHG	Disk Change	in
Pin 10	M02	Motor On 2	out
Pin 12	DIRC	Direction Select	out
Pin 14	STEP	Step	out
Pin 16	WD	Write Data	out
Pin 17	GND	Signal grounds	
Pin 18	WE	Write Enable	out
Pin 19	GND	Signal grounds	
Pin 20	TRKO	Track 0	in
Pin 21	GND	Signal grounds	
Pin 22	WP	Write Protect	in
Pin 23	GND	Signal grounds	
Pin 24	RDD	Read Data	in
Pin 25	GND	Signal grounds	
Pin 26	HS	Head Select	out

J15 PC/104 BUS interface

Pin	A:	B:	C:	D:
0			Ground	Ground
1	IOCHCK	Ground	SBHE	MEMCS16
2	SD7	RESET	LA23	IOCS16
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	NC	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	(-12V)	LA18	IRQ14
8	SD1	0WS	LA17	DACK0
9	SD0	+12V	MEMR	DRQ0
10	IOCHRDY	Ground NC	MEMW	DACK5
11	AEN	SMEMW	SD8	DRQ5
12	SA19	SMEMR	SD9	DACK6
13	SA18	SIOW	SD10	DRQ6
14	SA17	SIOR	SD11	DACK7
15	SA16	DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5 Volt
17	SA14	DACK1	SD14	MASTER
18	SA13	DRQ1	SD15	Ground
19	SA12	REF	Ground	Ground
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5 Volt		
30	SA1	OSC		
31	SA0	Ground		
32	Ground	Ground		

J16 Sound/Audio Port

Pin	Signal	Pin	Signal
1	Input_CD_L	2	GND
3	Input_CD_R	4	Input_AUX_L
5	GND	6	Input_AUX_R
7	Input_Line_L	8	GND
9	Input_Line_R	10	GND
11	Input_MIC 1	12	GND
13	Input_MIC 2	14	Input Mono
15	Output Front / Line Left	16	GND
17	Output Front / Line Right	18	GND
19	Output Surround Left	20	GND
21	Output Surround Right	22	GND
23	Output_Center	24	GND
25	Output_Subwoofer	26	GND
27	SPDIF Digital Output	28	Jack Sense 0 Input
29	Jack Sense 1 Input	30	Jack Sense 2 Input

J17 10/100 BASE-T interface Connector

J17 Pin *	Signal
Pin 1	= TX-
Pin 2	= TX+
Pin 3	= RX-
Pin 4	= RX+
Pin 5	= Activity LED
Pin 6	= BAT input 3.0-3.6V
Pin 7	= GND
Pin 8	= VCC 3.3V
Pin 9	= Speed LED
Pin 10	= Link LED

At the J17, the LAN-Interface board including the LAN-Transformator and the Lithium RTC-Battery (for backup) must be connected.

J18 PC/104+ BUS Interface

Pin	A	B	C	D
1	GND/5.0V KEY2	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY2

Notes:

1. The shaded area denotes power or ground signals.
2. The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. It is recommended that both KEY pins (A1 and D30) be electrically connected to GND for shielding. **DLAG boards have them as NC (not connected).**

Onboard used signals (not for external use):

IRQ3, IRQ4	COM1 /2
IRQ5	Sound
IRQ7	LPT1
IRQ6	FD
IRQ14	HD
IRQ12	PS/2 Mouse
IRQ13	Coprocessor
TC	FD
DACK2 and DRQ2	FD

J19 Power supply

Pin	Signal	Pin	Signal
1	= GND	2	= VCCSUS +5Volt Input Supply
3	= NC	4	= (+12V input)
5	= NC	6	= PWR_BTN#
7	= GND	8	= VCCSUS +5Volt Input Supply

VCCSUS = 5Volt Main Supply Input

X1 LCD TFT Interface (Flat Panel sSignals)

Pin	Signal	TFT 18 Bit	TFT 24 Bit
1	FPM (out)	LDE	LDE
2	CRT-Vert.Synch	VSYNC	VSYNC
3	Enable BKL (TTL out)		
4	CRT: Horiz. Synch	HSYNC	HSYNC
5	VCC 3.3V		
6	Ground		
7	NC		
8	Shift Clock	CKL	CKL
9	Enable VDD (TTL out)	ENLVDD	ENLVDD
10	FP0		Blue 0
11	FP1		Blue 1
12	FP2	Blue 0	Blue 2
13	FP3	Blue 1	Blue 3
14	FP4	Blue 2	Blue 4
15	FP5	Blue 3	Blue 5
16	FP6	Blue 4	Blue 6
17	FP7	Blue 5	Blue 7
18	FP8		Green 0
19	FP9		Green 1
20	FP10	Green 0	Green 2
21	FP11	Green 1	Green 3
22	FP12	Green 2	Green 4
23	FP13	Green 3	Green 5
24	FP14	Green 4	Green 6
25	FP15	Green 5	Green 7
26	Ground		
27	FP16		Red 0
28	FP17		Red 1
29	FP18	Red 0	Red 2
30	FP19	Red 1	Red 3
31	FP20	Red 2	Red 4
32	FP21	Red 3	Red 5
33	FP22	Red 4	Red 6
34	FP23	Red 5	Red 7
35	NC		
36	NC		
37	NC		
38	NC		
39	NC		
40	NC		
41	Ground		
42	NC		
43	+5Volt Output		
44	+12V Output		

12. INDEX

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